



Get Off the Bus and Call A TAXI

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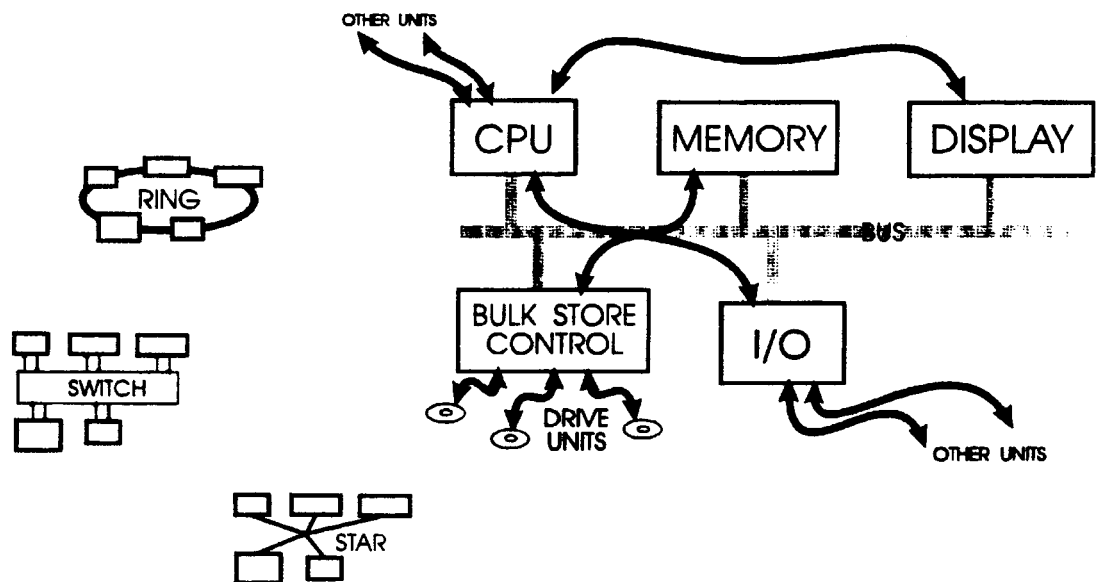


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GET OFF THE BUS AND CALL A TAXI

BUS INTERCONNECTS CAUSE COMMUNICATION BOTTLE-NECKS

TAXI™ LINKS CREATE PRIVATE SERIAL DATA CHANNELS



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PRIVATE SERIAL LINK ~~PROBLEMS~~ Challenges

SYSTEM ARCHITECTURE COMPATIBILITY

SERIAL LINK BANDWIDTH

INTEGRATION OF CLOCK GENERATION & RECOVERY

MANY DATA TRANSMISSION RATES

APPROPRIATE INTERCONNECT MEDIA & INTERFACE

TECHNOLOGY FOR CHIP DESIGN & MANUFACTURE

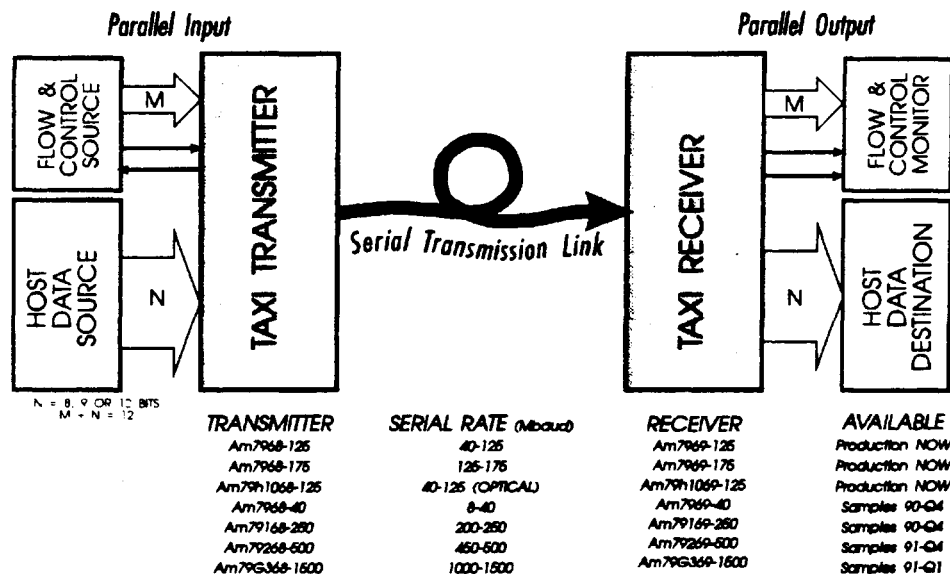
MINIMUM BOARD SPACE REQUIREMENT

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TAXIchip™ SYSTEM BLOCK DIAGRAM

Transparent Aynchronous Xmitter/Receiver Interface

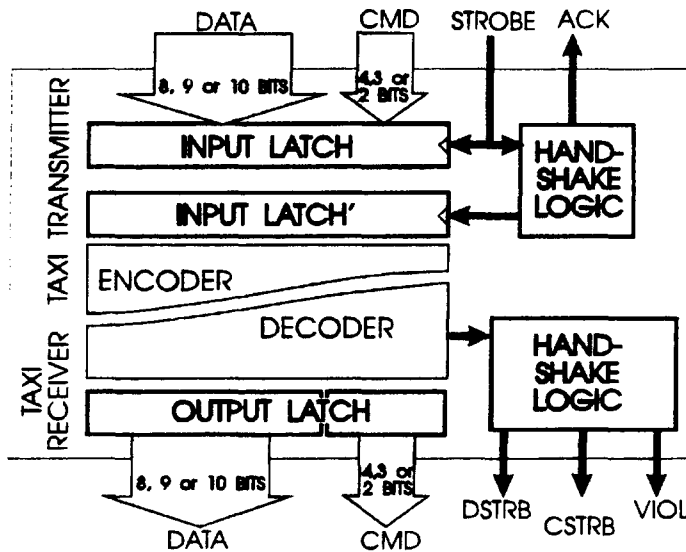


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TAXI PARALLEL INTERFACE

SIMPLE TO USE AS AN OCTAL REGISTER
 AUTOMATIC MUX/DEMUX DATA & COMMAND



Am7968/69-125
 0 - 12.5 Mbytes/sec
 TTL INTERFACE
 ASYNC or SYNC INTERFACE
 AUTOMATIC 'BYTE STUFFING'
 CODE VIOLATION INDICATOR

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TAXI CODES FACILITATE DATA TRANSFERS

ENCODER EFFICIENCY DETERMINES BANDWIDTH REQUIREMENT
 'OUT-BAND-SIGNALS' ENHANCE LINK BANDWIDTH
 CODE CHARACTERISTICS DEFINE LINK LIMITATIONS

REQUIREMENT

GROUP CODED & NRZI
 1 = 'TRANSITION' 0 = 'NO TRANSITION'
 RUN LENGTH 4 or LESS
 USE 'LOWEST' OFFSET AVAILABLE
 NO ALIAS SYNC WITH LEGAL DATA
 MAXIMIZE ERROR DETECTION

RESULT

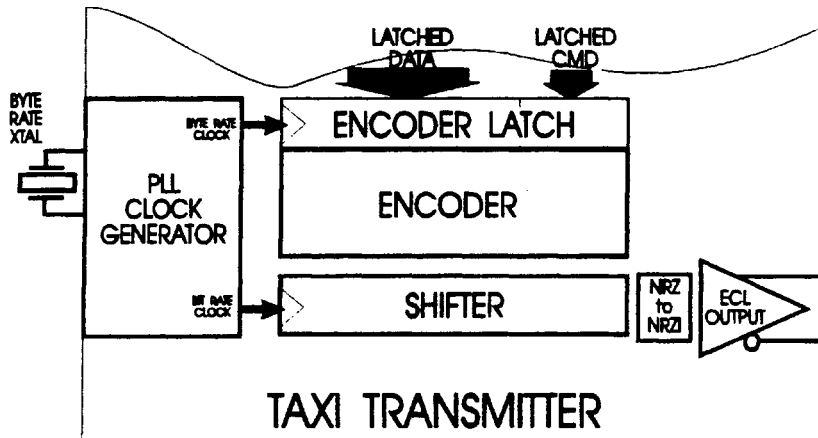
4B/5B & 5B/6B CODES ≤20% OVERHEAD
 8, 9, 10 BIT DATA BYTES
 4, 3, 2 BIT COMMAND SYMBOLS
 CODES SUPPORT NETWORK STANDARDS

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TAXI SERIAL OUTPUT

INTERNAL PLL GENERATES BIT CLOCK FROM EXTERNAL BYTE FREQUENCY
ENCODER ASSURES EFFICIENT DATA TRANSFER WITH HIGH TRANSITION DENSITY



Am7968-125

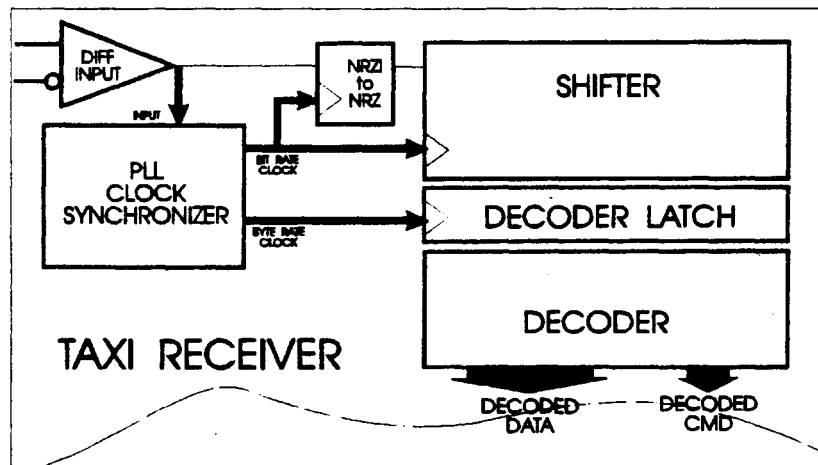
BUILT IN. BYTE RATE XTAL OSC
TTL COMPATIBLE BYTE RATE INPUT
4-12.5 Mbytes/sec
AUTOMATIC SYNC INSERTION
100K ECL OUTPUTS (+5v REF)
INTEGRATED MULTIPLIER PLL
40-125 Mbaud
NO EXTERNAL COMPONENTS

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TAXI SERIAL INPUT

INTERNAL PLL SYNCHRONIZES BIT CLOCK WITH INCOMING SERIAL STREAM
DECODER SEPARATES DATA FROM COMMAND AND FLAGS ERRORS



Am7969-125

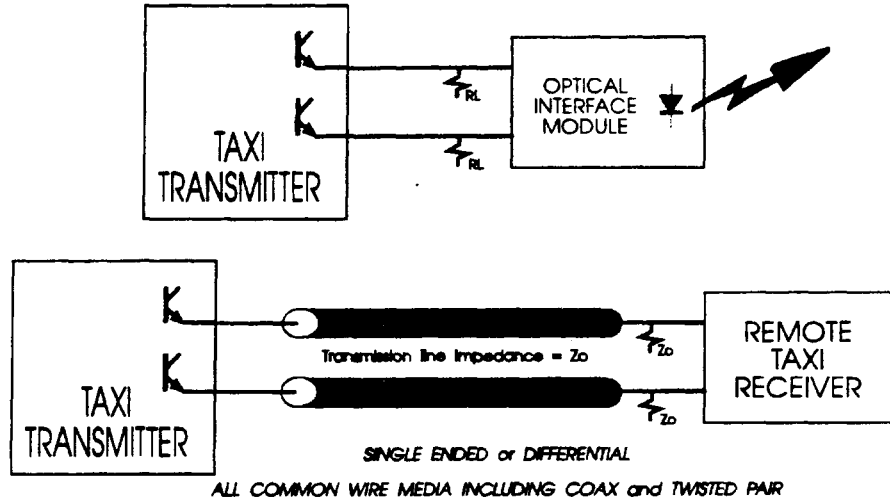
INTEGRATED PLL
40-125 Mbaud
NO EXTERNAL COMPONENTS
WIDE JITTER TOLERANCE (40%/BIT)
AUTOMATIC BYTE FRAMING
DETECTS CODE VIOLATIONS

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TAXI SERIAL INTERFACE

ECL 100K OUTPUTS INTERFACE TO STANDARD OPTICAL MODULES
 LOW IMPEDANCE DRIVERS CAN DRIVE LONG TRANSMISSION LINES

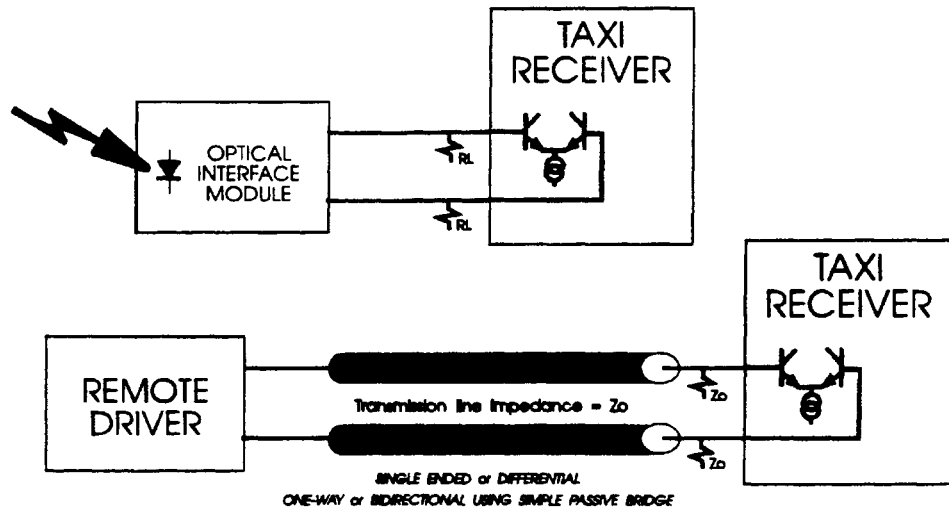


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TAXI SERIAL INTERFACE

DIFFERENTIAL INPUT COMPATIBLE WITH STANDARD OPTICAL MODULES
 HIGH SENSITIVITY AND WIDE COMMON MODE RANGE ENCOURAGE WIRE INTERCONNECT

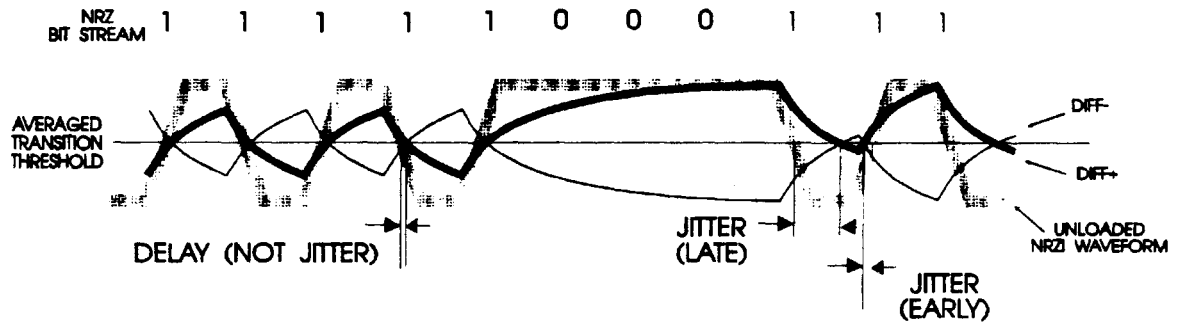


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LINK LENGTH LIMIT

BANDWIDTH LIMITED LINKS (COAX) CAUSE JITTER IN NORMAL DATA
JITTER LIMITS THE LINK LENGTH BEFORE THE AMPLITUDE LIMIT

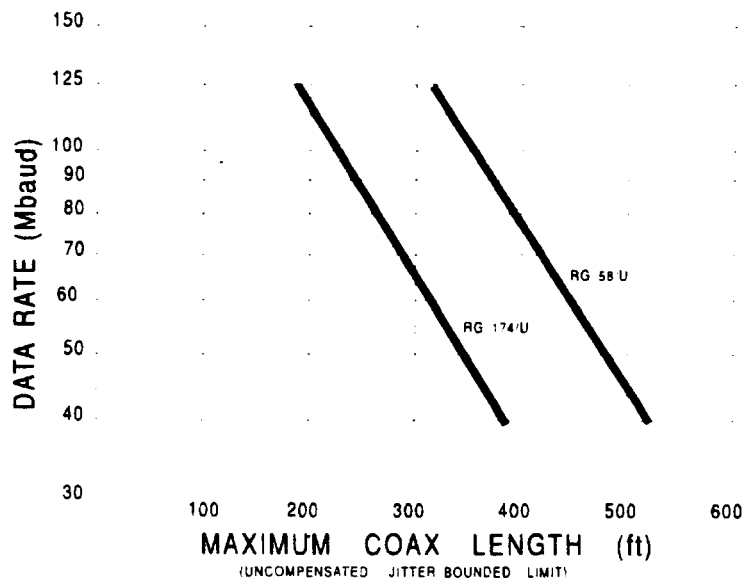


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TAXIchip LINE LENGTH

TRANSMISSION LINE CHARACTERISTICS LIMIT LENGTH
EACH TYPE HAS DIFFERENT ECONOMIC & PERFORMANCE TRADEOFFS

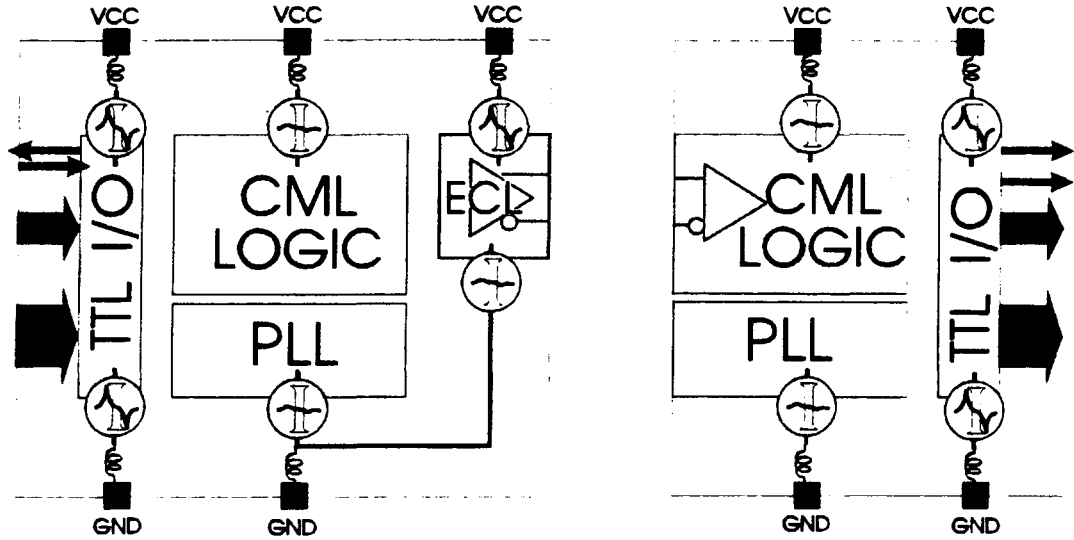


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TAXIchip POWER BUS PARTITION

TTL & ECL I/O NOISE ISOLATED FROM CORE BY BUS SEPARATION
 INTERFACES BETWEEN I/O AND INTERNAL LOGIC & PLL ARE DIFFERENTIAL
 INTERNAL CURRENT TRANSIENTS CREATE NOISE VOLTAGES IN LEAD INDUCTANCE
 CML AND PLL CIRCUITS CAUSE MINIMAL INTERNAL NOISE

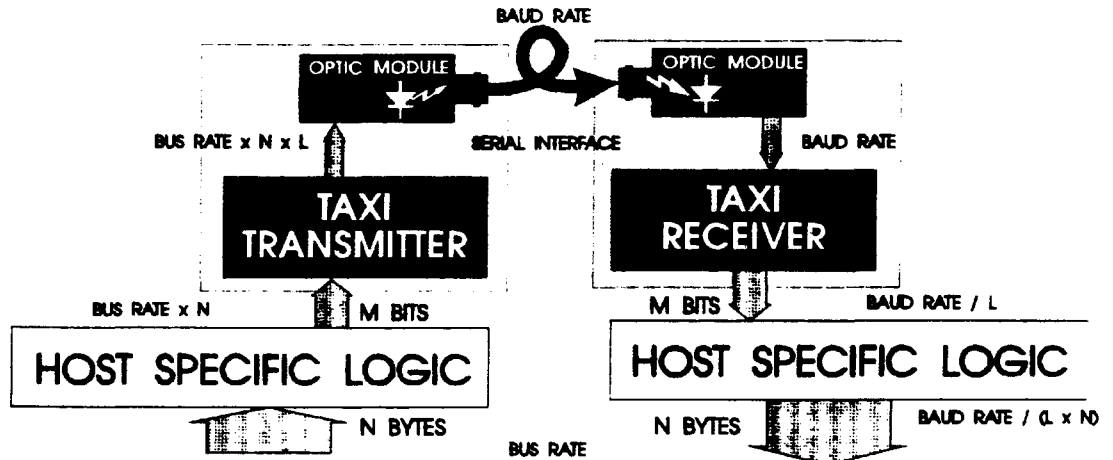


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TAXIchip PRODUCT PARTITION

REDUCE DATA CORRUPTION CAUSED BY CROSSTALK
 MINIMIZE INTERFACE DATA RATE
 SELECT BLOCKS FOR EFFICIENT, MANUFACTURABLE INTEGRATION
 MINIMIZE CHIP COUNT AND INTERFACE PIN COUNT



N=#BYTES/WORD
 M=#BITS/BYTE
 L=M+2 (BITS/ENCODED BYTE)

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TAXIchip SERIAL LINK SOLUTIONS

FLEXIBLE SYSTEM INTERFACE

DRIVES TRANSMISSION LINES or OPTICAL MODULES

PLLs WITH NO EXTERNAL COMPONENTS

INTERNAL BIT RATE CLOCK GENERATOR

INTEGRATED CLOCK/DATA RECOVERY PLL

WIDE FREQUENCY RANGE

MATURE IC TECHNOLOGY FOR MANUFACTURABILITY

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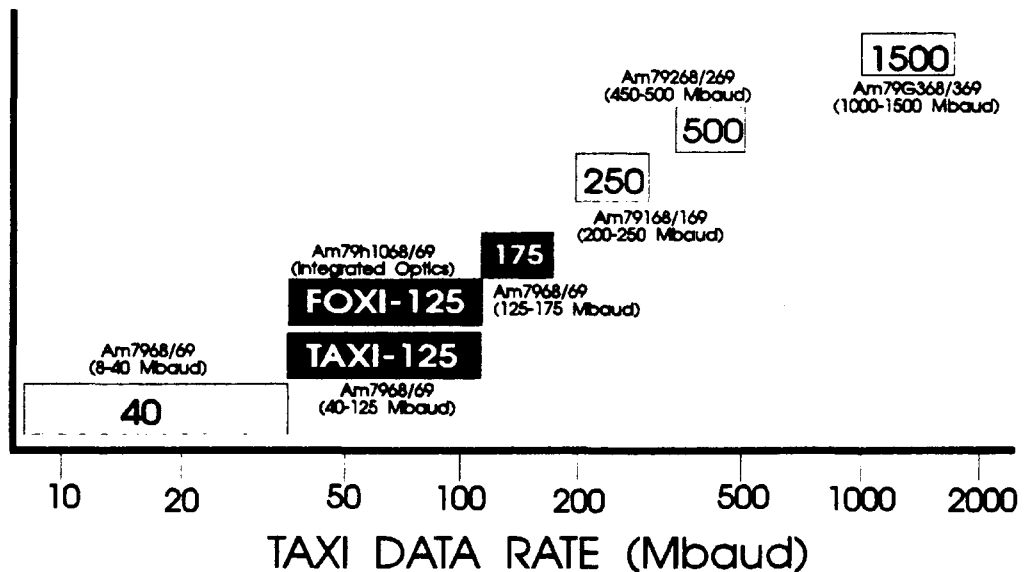
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TAXIchip SPEED LIMITS

TAXI_s ADDRESS SPECIFIC DATA COMMUNICATION REQUIREMENTS

SPEEDS DEFINED BY INTERFACE LIMITATIONS AND SYSTEM CONVENTIONS

PRODUCTS PARTITIONED FOR COST EFFECTIVE SYSTEM SOLUTIONS



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