DataWave
A Data-Driven Video Signal Array Processor

Ulrich Schmidt
ITT Intermetall, Freiburg, Germany

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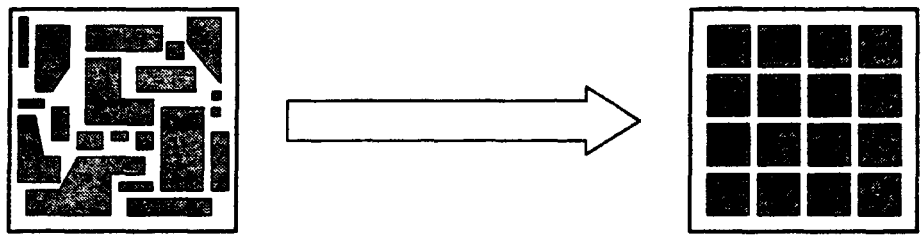
- Architecture of the Data-Driven Array Processor
- Application Examples
- A Look into the Future

Hardwired vs. Programmable Solutions



Arguments for "structured hardware"

- Transistors/chip: 1 million today (1990), 100 million tomorrow (2000)
- Adding dedicated functions adds only marginal value
- Dedicated functions waste chip area if not needed
- Do not dedicate at design time, dedicate at run time!
- Program changes are done faster than hardware changes
- Regular structures are easier to design and test than irregular structures

Application Areas

- 3 – 144 MHz video signals
- Today: NTSC / PAL / SECAM / D2-MAC
- Tomorrow: EDTV / IDTV / HDTV
- Real-time motion-compensated scan rate conversion
- Image compression/decompression (DCT, sub-band)
- Graphics + Video
- Image analysis (robot vision)

- ▸ Required computational throughput > 10 GOPS
- ▸ Required I/O throughput > 100 MByte/s

Architecture of the Data-Driven Array Processor

Architecture

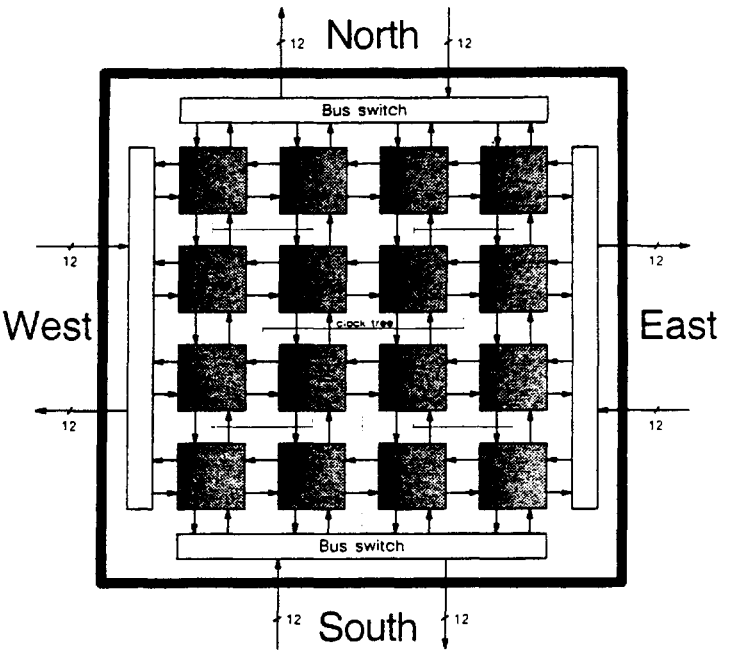
- 16 mesh-connected cells
- Multiple instructions, multiple data
- 12-bit word length

Technology

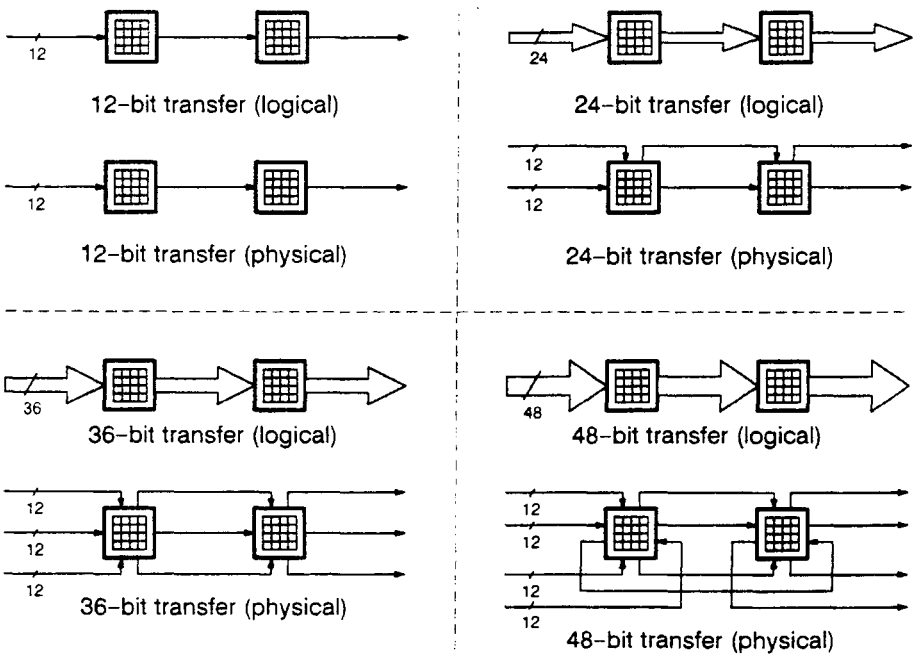
- 0.8 µm CMOS
- 125 MHz on-chip (8 ns)
- 62.5 MHz off-chip (16 ns)
- 124 pins

Performance

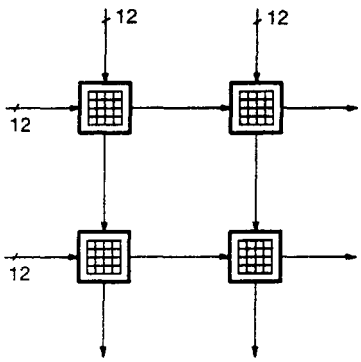
- 4000 MOPS
- 750 MByte/s chip I/O
- 1125 MByte/s cell I/O



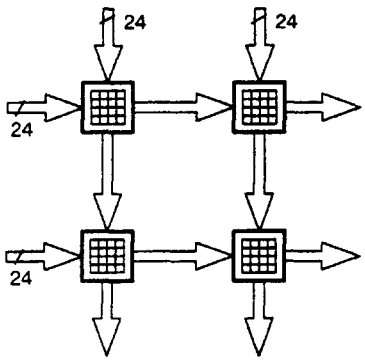
One-dimensional Cascading of Array Processors



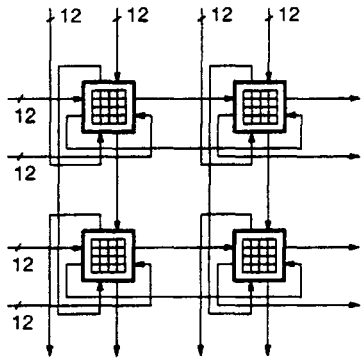
Two-dimensional Cascading of Array Processors



12-bit transfer



24-bit transfer (logical)



24-bit transfer (physical)

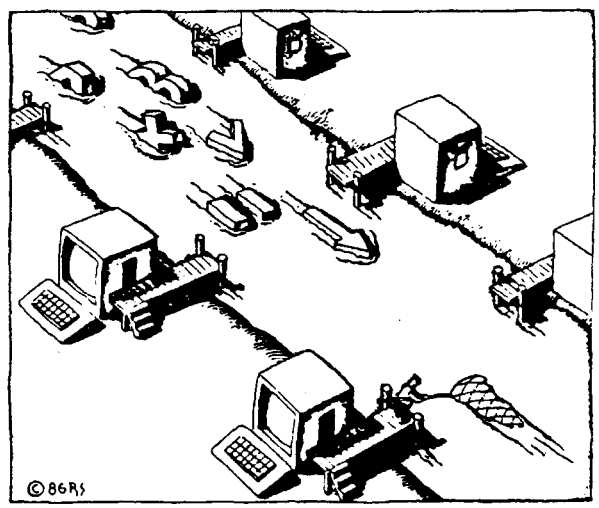
Data Flow Communication

Architecture

- *Sequencing* instead of *timing*
- *Data-driven* instead of *clock-driven*
- Cells "freeze" if neighbours are not ready
- Local changes do not cause global effects
- Executes statically scheduled data flow programs

Implementation

- Common 125 MHz clock
- Self-timed asynchronous handshake protocol
- "Freeze" by automatic insertion of wait cycles
- Completely transparent: no polling, no interrupts
- 1 cycle / intercell transfer
- 2 cycles / interchip transfer



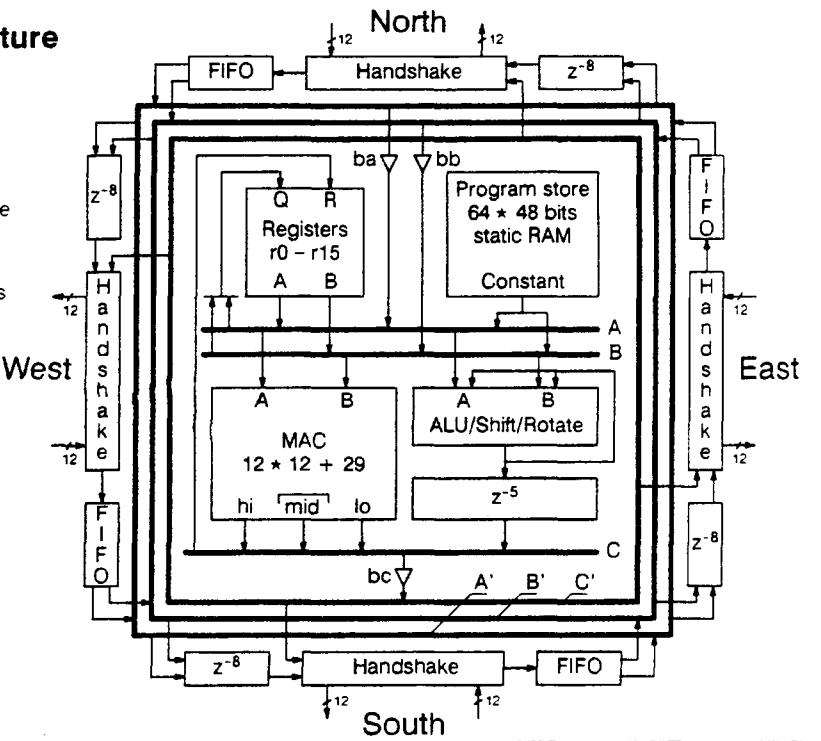
Cell Architecture

Superscalar RISC Architecture

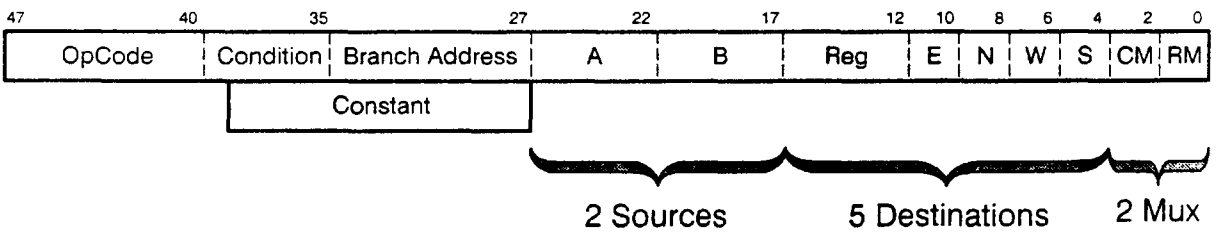
- Wallace-tree multiplier
- Multiply-Accumulate in every cycle
- 3 ring buses, 3 core buses
- 64 instructions in static RAM, 48 bits wide
- Four-port register file, 16 registers
- Deep pipeline with short feed-back loops
- 12-bit ALU, 1 cycle delay
- n 1-bit shifts/rotates in n cycles

Intercell Communication

- Up to 6 cell-to-cell transfers every cycle
- Self-timed handshake with FIFOs
- Dual-port circular buffers (8 words)
- Automatic pipeline freeze when waiting



Instruction Format



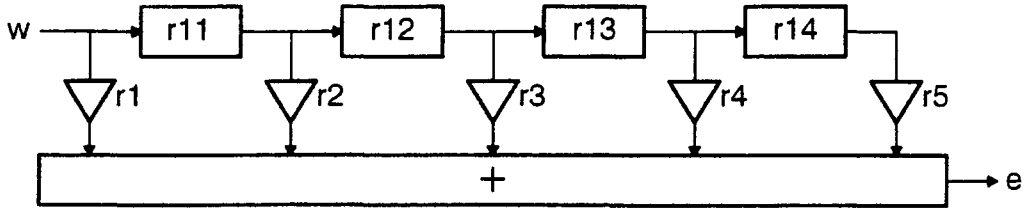
Large Instruction Word:

- Arithmetic + Intercell Communication + Register Transfers + Branches
- Horizontally coded
- No special load/store instructions: communication ports are treated like registers
- Branches are delayed by 3 cycles

Example:

n = s = r13 = acc + w * r12, e = w, bra Label

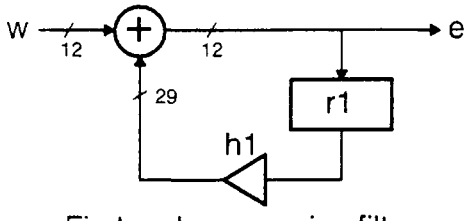
FIR Filter




```
Loop   acc =         r1 * w,    r11 = w
       acc = acc +   r2 * r11,  r12 = r11,  bra Loop
       acc = acc +   r3 * r12,  r13 = r12
       acc = acc +   r4 * r13,  r14 = r13
       e   = acc +   r5 * r14
```

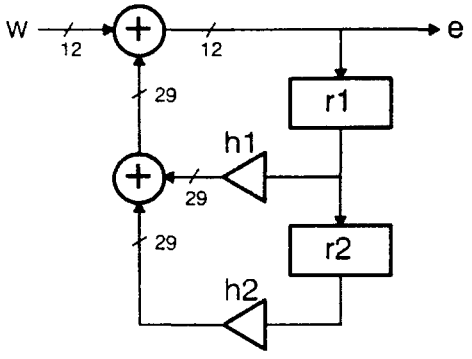
Note: 12-bit I/O, 29-bit accumulation
One FIR tap per cycle
Loop diameter = clock rate / sample rate
Sustained performance: 250 MOPS

IIR Filters



First-order recursive filter

```
Loop   mid     = w
       e = r1  = acc + h1 * r1
       nop
       bra Loop
       nop              ; delay slot 1
       nop              ; delay slot 2
       nop              ; delay slot 3
```



Second-order recursive filter

```
Loop   mid     = w
       acc     = acc + h2 * r2
       e = r1  = acc + h1 * r1
       r2      = r1, bra Loop
       nop
       nop
       nop
```

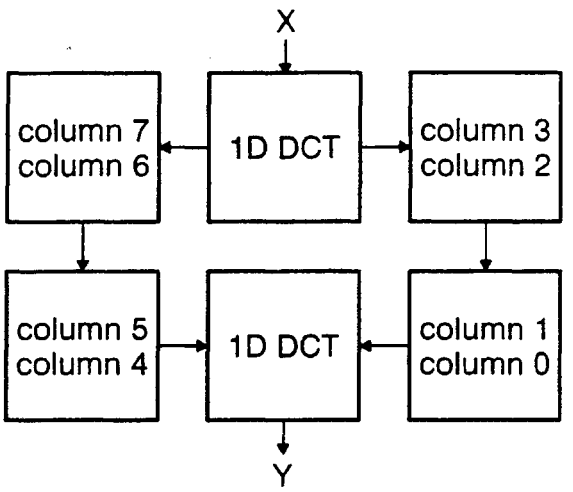
2D (8 * 8) Discrete Cosine Transform

Formula: $Y = DCT * (DCT * X)^T$

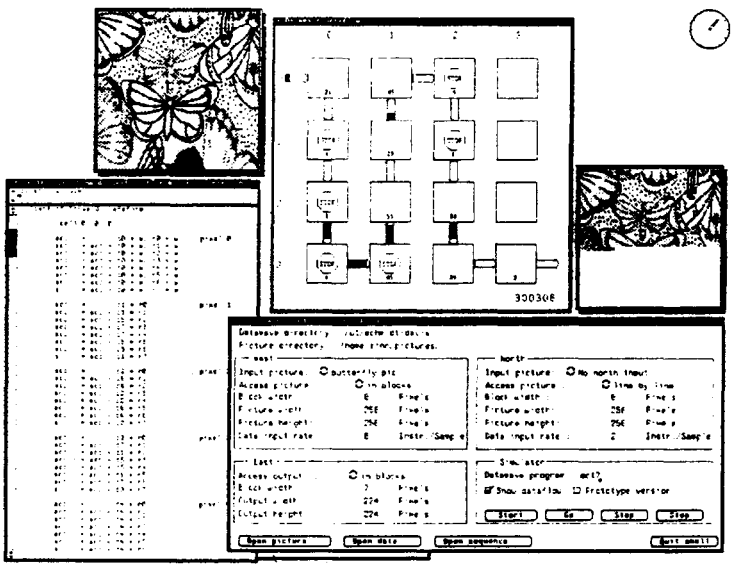
where X : (8 * 8) frame buffer region
DCT : (8 * 8) coefficient matrix

Assumptions:
- sample rate: 13.5 MHz
- clock rate: > = 108 MHz
- ** 8 cycles/sample

Transposition:
- Store in column order
- Read in row order

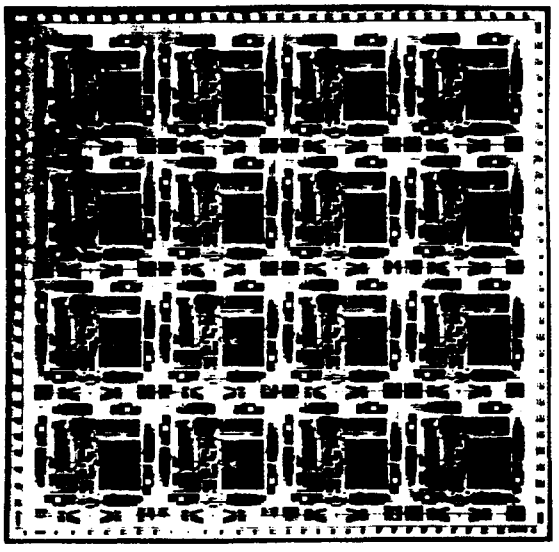


Simulation and Debugging Environment

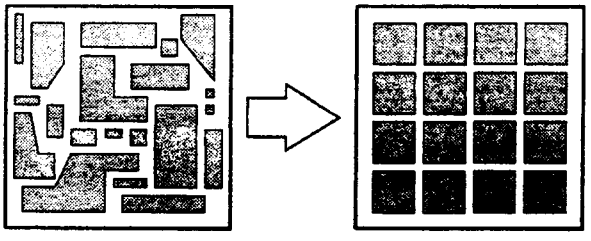


DataWave – Technical Data

- 0.8 micron double-metal CMOS
- 125 MHz clock
- 1.2 million transistors
- 150 mm^2 chip area
- 124 pins
- 8 W maximum power dissipation

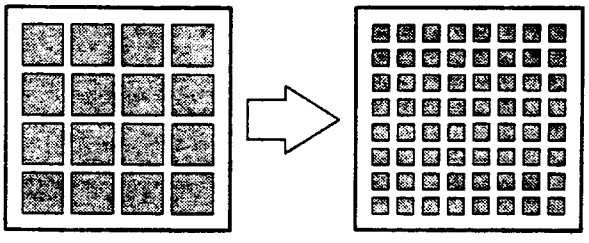


What we did ...



- Software for hardware
- Cellular array topology
- Process: 0.8 micron CMOS
- Density: 16 cells/chip
- Clock rate: 125 MHz
- Performance: 4 GOPS

... what we are going to do



- Software unchanged
- Array topology unchanged
- Process: 0.4 micron CMOS
- Density: 64 cells/chip
- Clock rate: 250 MHz
- Performance: 32 GOPS