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A 100 MHz Floating Point/  
Integer Processor

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A 100 MHz Floating Point/  
Integer Processor

- \* Introduction
- \* Overview
- \* Major blocks
- \* Testing
- \* Conclusion

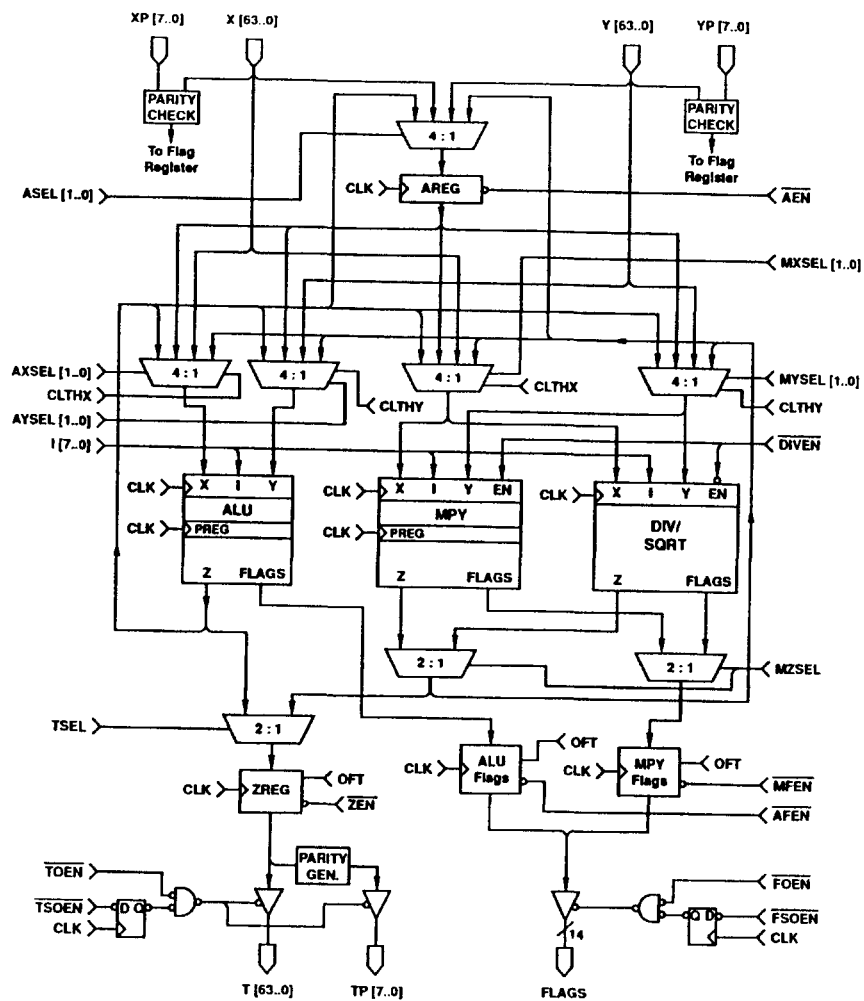
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## Features of the B3130

- \* Compatible with the B3110/B3120
- \* IEEE, DEC, and integer arithmetic
- \* 32- and 64-bit operands
- \* three 64-bit ports - 2 in, 1 out  
with programmable parity checking
- \* unpipelined operation at 50 MHz
- \* pipelined operation at 100 MHz
- \* three parallel functional blocks  
operate simultaneously:
  - ALU
  - multiplier
  - divide / square root
- \* 10KH, 100KH, or TTL I/O

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B3130 Block Diagram

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## Layout

- \* functional blocks are stacked and connected through the datapaths
- \* rectangular die:
  - increases pins to die area ratio
  - simplifies power distribution
- \* 3 layer metal with 4, 4, and 8 um pitch
- \* ECL internal logic, metal programmable I/O
- \* Major supply buses supply all core current to control droops
- \* Supply widths are IR drop limited
- \* 200K transistors, 120K resistors
- \* die size: 9 mm x 18 mm
- \* Scalable to BIT's next generation process

TTL:	pads	pins
VEE	27	24
VEED	21	30
VCC	33	56
VCCD	43	
inputs	190	190
outputs	87	87

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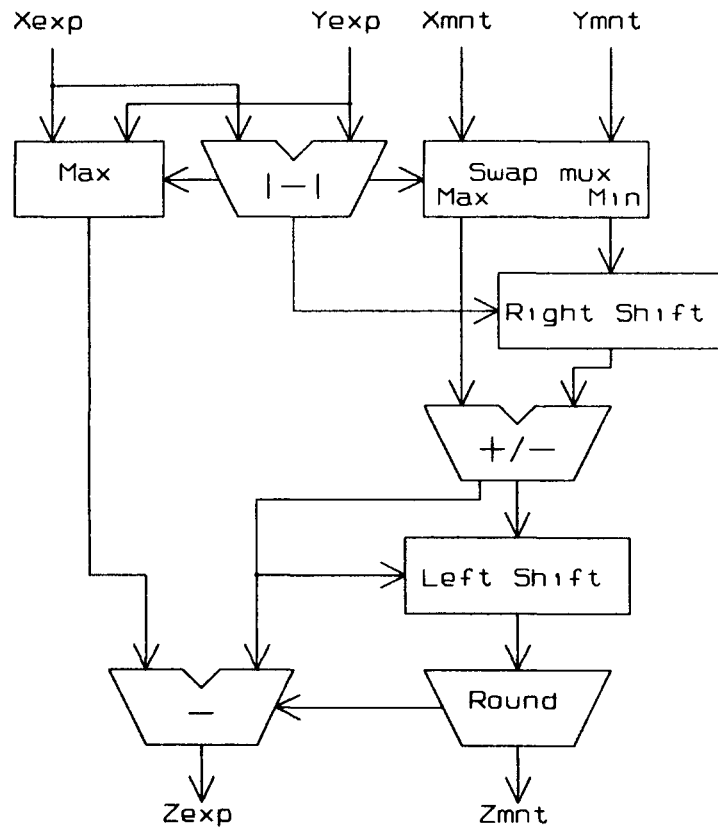
## ALU

- \* Floating point operations:
  - add, subtract, compare, round, min, max, absolute value, negate, scale
- \* Integer operations:
  - add, subtract, compare, min, max, absolute value, negate, shift, booleans
- \* Conversions between all floating and integer formats
- \* 64-bit wide datapath includes:
  - right shifter
  - Ling adder
  - left shifter
- \* Integer datapaths are a subset of floating point
  - only rotate is unsupported
  - dedicated datapaths would be faster, but would cost area, power, and complexity

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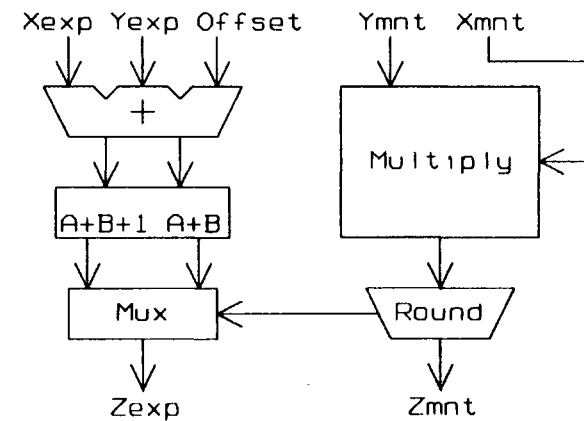
## Floating Point Alu



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## Floating Point Multiplier

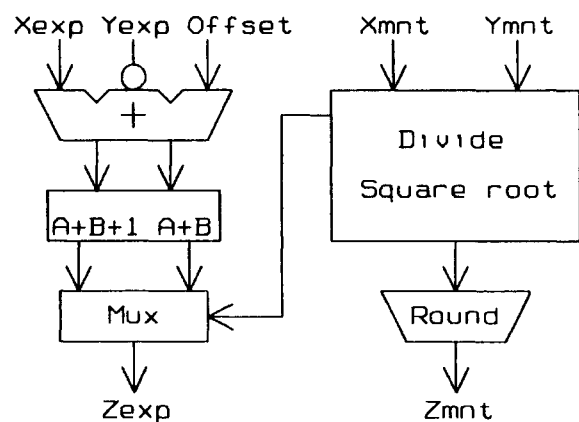
- \* Floating point multiplication
- \* Integer multiplication
  - signed and unsigned operands
  - 8-, 16-, and 32-bit operands
- \* Bit reverse
- \* full 54 x 54 multiplier array
  - smaller array would limit dp performance
  - a 64 x 64 array would be 50% larger
- \* conditional exponent and flag generation
- \* product sticky bits included in scan chain



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## Floating Point Divide/Square Root

- \* Floating point division and square root
- \* Integer division and remainder
- \* 64 bit integer multiply
  - returns low 64-bits and overflow flag
  - uses existing divide unit datapaths
- \* pseudo-combinatorial
  - 200 MHz internal oscillator (synchronized at the start of operations)
- \* floating point overflow and underflow flags are available quickly - limiting the costs of implementing precise exceptions



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## Testing

- \* 277 pins at 100 MHz
- \* single clock controls many registers
- \* internal feedback is limited
- \* all user visible registers are scanned
  - internals of the pseudo-combinatorial div/sqrt block are not scanned
- \* internal test points are scanned, e.g. multiplier product sticky bits
- \* extra hardware was added to overcome the testing difficulties

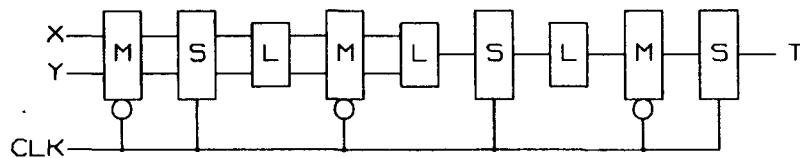
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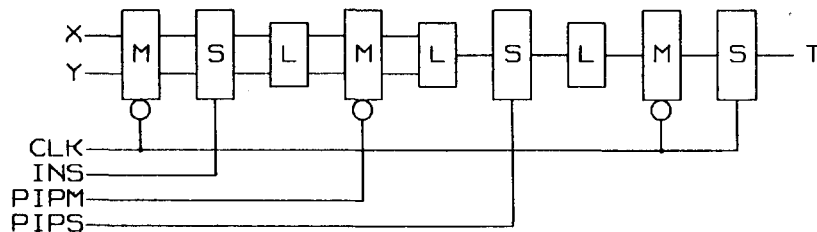
## Test Mode Features

- \* four separate clocks allow each of the on chip registers to be clocked independently
- \* data can be clocked through the part independent of the speed at which it is presented
- \* div/sqrt oscillator can be driven by four pins
  - 320 MHz clock requires 80 MHz inputs
  - single stepping and speed testing

### Normal Clocking



### Test Mode Clocking



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## Conclusion

- \* the B3130 is the world's fastest IEEE floating point arithmetic processor
  - 200 MFlops peak
  - 2.4 GByte/s data bandwidth
- \* suitable for vector or scalar use
- \* designed for testability

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