A 120 MFLOPS Floating Point Processor

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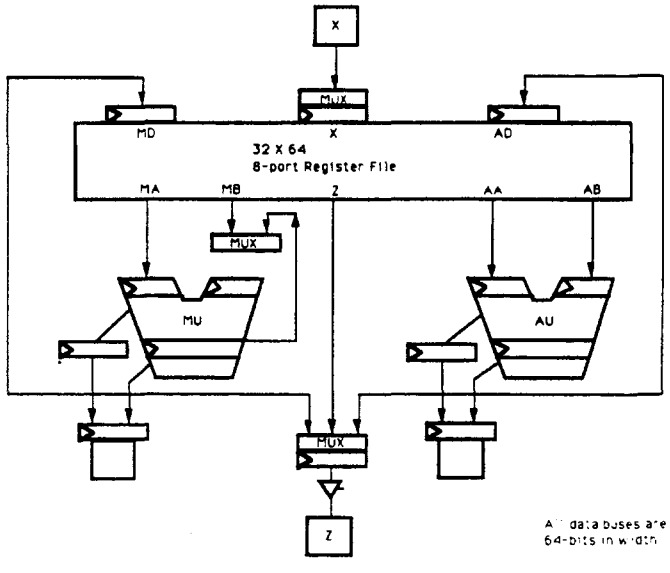
Agenda

- Project Goals
- Features
- Algorithms/Implementation
  - ALU
  - MPY
  - DSR
- Performance

Project Goals

- Versatile building block floating point processor
- 60 MHz operation with 0.8 micron CMOS
- High performance - low latency, high bandwidth
- Low power dissipation

Next-Generation Floating Point Processor Block Diagram



Features

- Two 64-bit I/O buses with byte-parity
- 60 MHz operation
- TTL output levels
- 370 pin PGA package
- Large 8 ported register file (32x64x8 or 64x32x8)
- Fully independent adder and multiplier and I/O operations

Features
(continued)

- Three cycle 32/64-bit Reg-to-Reg operation latency (except divide,sqrt)
- Full 32-bit integer functions
- IEEE 754 compatible single and double precision
- Direct min/max operations

Operation Times

Operation	R-to-R Latency	Bandwidth
FP ADD, SUB	3	1
FP MUL	3	1
INT MUL	3	1
FP SINGLE DIV	7	5
FP DOUBLE DIV	9	7
FP SINGLE SQRT	7	5
FP DOUBLE SQRT	10	8
F-->I	3	1
I-->F	3	1
FP compare	3	1
All other integer ops	3	1

ALU

- Multiple adders operating in parallel
- Correct results selected at the end of the operation
- Normal FPU add algorithm takes 6 operations
  1. Exponent compare
  2. Pre-alignment (right shift of fractions)
  3. Add/subtract
  4. Re-complement (if needed)
  5. Post-normalization (left shift of fraction)
  6. Exponent update

ALU
(continued)

- Parallel algorithm cuts operations in half

Case A

1. Exponent compare (pipe 1)
2. Pre-alignment (pipe 1)
3. Add/Subtract (pipe 2)

Case B

1. Subtract/re-complement (pipe 1)
2. Post-normalization
3. Exponent update (pipe 2)

MPY

- Full array of CSA enables double precision throughput at 1 result per cycle
- CSA connected in an arithmetic progression scheme, which approaches speed of full Wallace Tree at much reduced complexity (less CSA and interconnects)
- Multiply has 2 cycle latency and 1 cycle through-put for either single precision or double precision

DSR

- Uses polynomial approximation scheme for SP
- Uses quadratic convergence scheme for DP
- CSA array dynamically re-configurable to two half arrays
- Modified booth recoder that accepts inputs in carry-save form as well as 2's complement form

Chip Statistics

- 0.8 micron CMOS process
  - 356K transistors
  - 530 x 530 mils*
- 60 MHz operation**
  - 3 watts*
- 370 pin PGA package

* Estimated

** Simulated (typical process, worst case commercial operating conditions)

Chip Comparison

	Weitek Floating Point Processor	BIT B-2130-10*
Format	IEEE 754	IEEE 754, DEC
Reg File	64x32x8	n/a
	32x64x8	n/a
SP ALU (cycles)	2	2
DP ALU (cycles)	2	2
SP MPY (cycles)	2	2
DP MPY (cycles)	2	2
SP DIV, SQRT (cycles)	6	15,25
DP DIV, SQRT (cycles)	8,9	25,30
OPERATING FREQ	60 MHz	100 MHz
POWER (max)	3W	28W
Technology	0.8 micron CMOS	ECL

* B2130/B3130/B4130 advance information, Bipolar Integrated Technology Inc.