SILICON MULTICHIP MODULES

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AGENDA

LIMITATIONS OF SINGLE CHIP PACKAGING SOLUTIONS

nCHIP'S MCM (MULTICHIP MODULE) SOLUTION

AN MCM APPLICATION (ROSS TECHNOLOGY)

INCREASING CHIP I/O IS A MAJOR COST CONSIDERATION

- High performance packages cost 5-10¢/pin
  - A 400 pin IC package can cost more than $40
- More expensive PCBs (printed circuit boards) are required:
  - PCB interconnect density requirements increase as:
    Interconnect density ~ (# of chip terminals/chip pitch)
  - PCB cost increases rapidly with increasing interconnect density

HOT02

CAPACITANCE LIMITATIONS

- High performance, impedance controlled packages have high pin capacitance (5 - 8 pF/pin)
- PCB interconnect technology contributes
  - 3 - 4 pF/in
  - ~1 pF/plated through-hole
- "Capacitive" delay of interconnect in CMOS systems (PCB) is often more than 4 ns

Hot03

WHEN DOES LEAD INDUCTANCE BECOME A PROBLEM?

The voltage drop on a package lead is:

$$\Delta V = -L_{lead}\, di/dt \sim -L_{lead}\,(V_o/Z_o t_{rise})$$

If you want $\Delta V/V_o = 0.1$ and $Z_o = 50\Omega$, then:

t_{rise} (ns)	L_{lead} (nH)
1.0	5.0
0.5	2.5
0.2	1.0

If you have N lines switching at once: $\Delta V = -N\, L_{power} di/dt$

For N=40: t_{rise} (ns)	L_{power} (nH)
1.0	0.12
0.5	0.06
0.2	0.025

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LEAD INDUCTANCE FOR SINGLE-CHIP MODULES (180 I/O)*

	Wirebonded Pin Grid Array	TAB Package
Substrate Size (mm^2)	36	30
Lead Inductance (nH)		
(Min.)	7.0	8.5
(Max.)	24	12.5

Package lead inductance poses substantial performance limitations

* From Microelectronics Packaging Handbook, Van Nostrand, Reinhold, 1989

Hot05

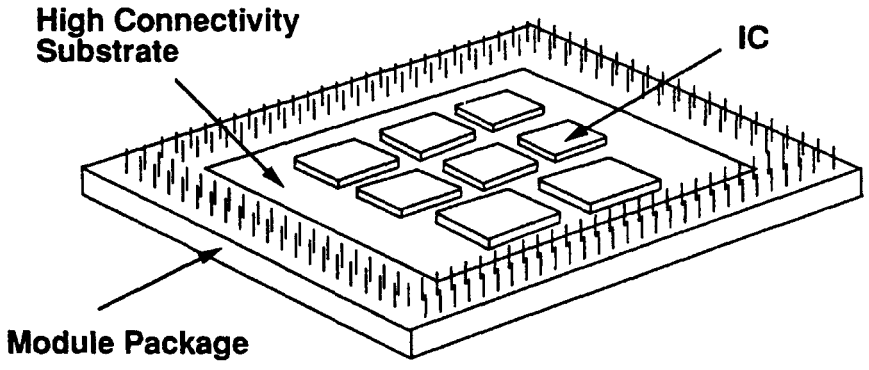
SINGLE-CHIP PACKAGING LIMITATIONS

- Single-chip packaging solutions have a major effect on system performance and cost
  - Capacitance, inductance, and long interconnect distances substantially reduce system performance
  - High pin count ICs require expensive packages and PCBs

Solution: Eliminate the chip package and reduce chip-to-chip spacing

WHAT IS A MULTICHIP MODULE (MCM)?

A collection of die attached to a high density interconnect structure which functions as a single integrated circuit.



MCM ADVANTAGES

- Supports high pin count ICs without cost or performance penalty
- Improves performance
  - Low inductance (less than 2 nH/pin) and capacitance (better than 4x reduction)
  - Packaging delays for CMOS are reduced by at least 4 ns in most applications
  - Packaging delays for ECL are reduced by at least 2 ns in most applications
- Higher packing density (5 - 20x area reduction in most applications)

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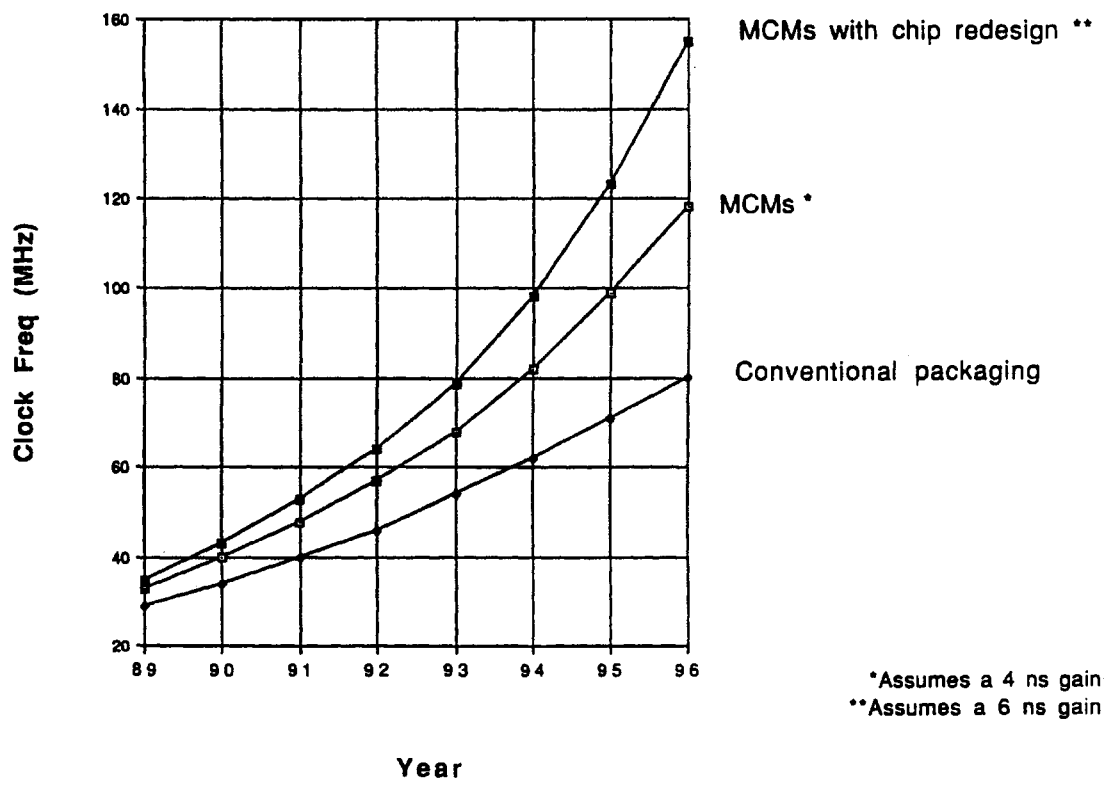
MICROPROCESSOR PERFORMANCE



*Assumes a 4 ns gain
**Assumes a 6 ns gain

nCHIP MULTICHIP MODULE TECHNOLOGY

- **Interconnection Substrate**

  Base material - Silicon
  Dielectric - SiO_2
  Metallization - Aluminum or Copper
  Passives (R, C)

- **Assembly**

  Wire bond
  Flip chip (1991)

- **Package (Module Carrier)**

  Ceramic
  Low cost non-hermetic (1991)

- **Cooling**

  Air
  Liquid

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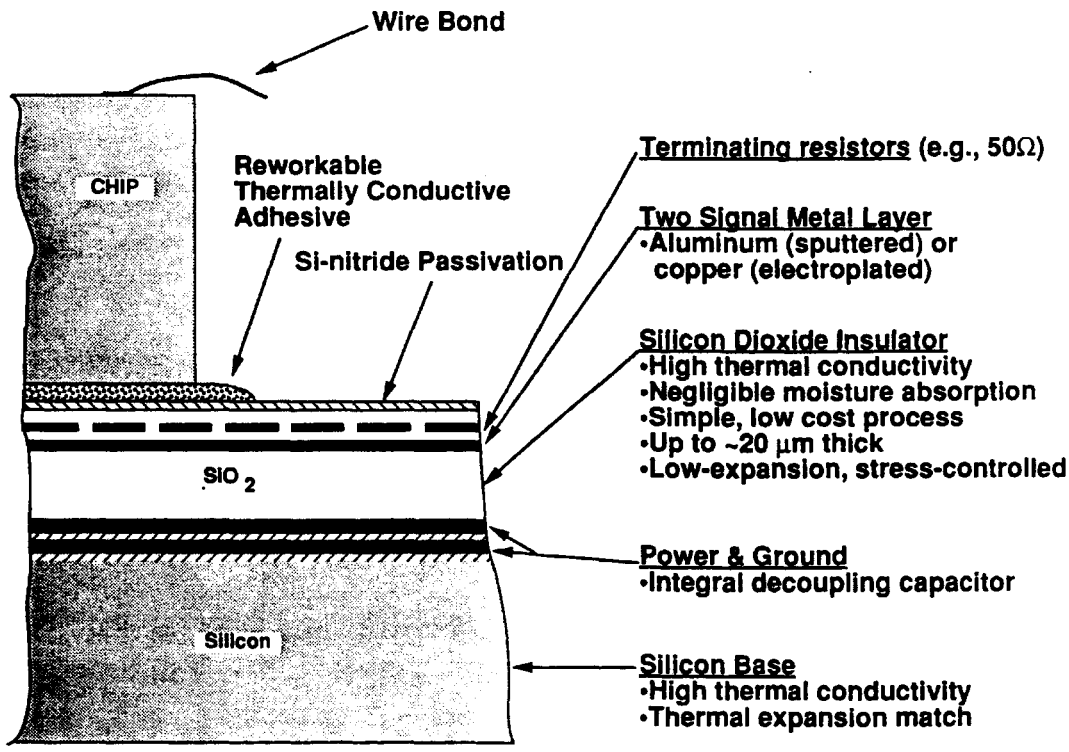
nCHIP SILICON CIRCUIT BOARD



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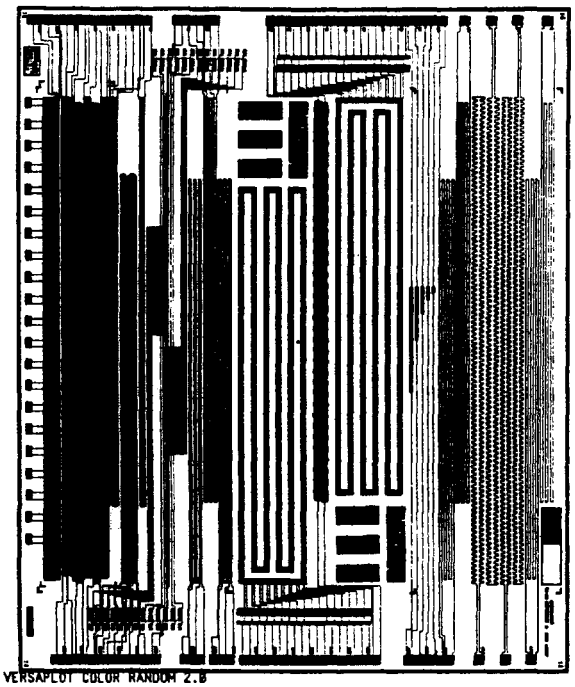
nCHIP SUBSTRATE CHARACTERISTICS

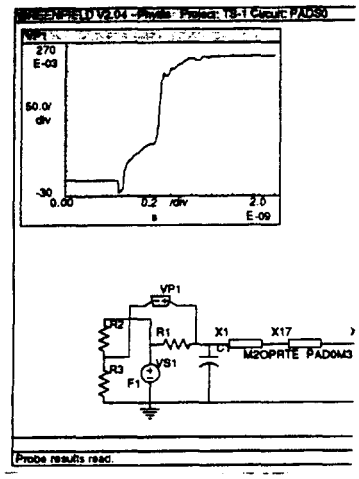
		Type D	Type C		Type E	
Number of Signal Layers		2	2		2	
Number of Power Layers		2	2		2-3	
Max Wiring Density (in/in^2)		2000	1360		1000	
Metal Pitch (μm)		25	37.5		50	
Conductive Metal		Aluminum	Copper		Copper	
Dielectric Constant		3.5	3.5	IsoStrip™ 1.9	3.5	IsoStrip™ 1.9
Capacitance/nominal width (pF/cm)		1.2	1.2	0.65	1.26	0.69
Resistance	nominal width (Ω/cm)	15	3.8		1.6-2.2	
	1 mil width (Ω/cm)	5.9	2.3		1.0-1.4	
Impedance/nominal width (Ω)		50	50	70	50	70

TEST SUBSTRATE

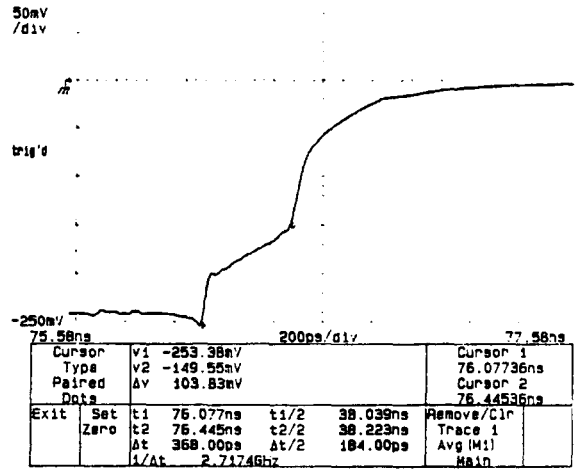


- Test substrate size is 2.73 cm x 2.21 cm and has 120 signal pads and 93 power and ground pads
- Verifies Electrical, Technology & Assembly characterisitcs and limits
- Variations of the basic design rules were implemented on three different substrates
- 16 structures for delay and crosstalk measurement for both the interconnect layers
- 12 structures which stress various aspects of the process technology like step coverage, minimum feature sizes, minimum spacing, etc.
- 8 different structures, including *test die,* which are used for die attach and wire bonding tests

DELAY - M3 2cm LINE



Type D SiCB



- **Type D**
  Simulated delay of 2 cm M3 line is 175 ps
  Measured delay of 2 cm line is 184 ps
- **Type C simulated delay of 2 cm M3 line is 155 ps**

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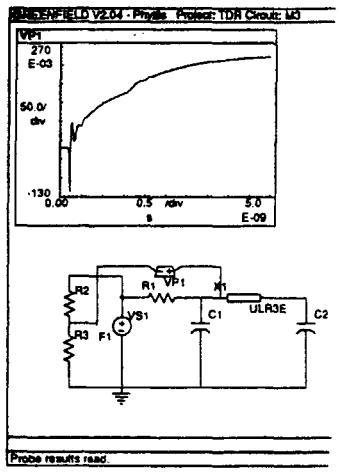
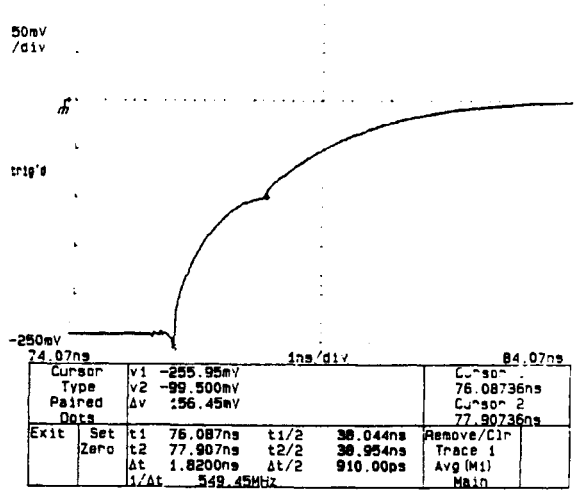
DELAY - M3 10cm LINE

Type D SiCB





- **Type D**
  Simulated delay of 10 cm M3 line is 850 ps
  Measured delay of 10 cm line is 910 ps
- **Type C simulated delay of 10 cm M3 line is 692 ps**

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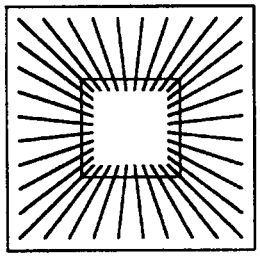
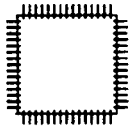
nCHIP WIRE BONDS HAVE LOW INDUCTANCE

In conventional IC packages, the wire bonds are used as space transformers.



- Wire bond lengths up to ~180 mils
- Resistance, inductance, and "sag" a problem
- Wire diameters must be large (~1.3 mil)

The nCHIP bond pad pitch is matched to the IC chip.



- Wire bond lengths 40-50 mils
- Inductance is low (1.2nH)
- Bond pitch can be fine (4 mils)

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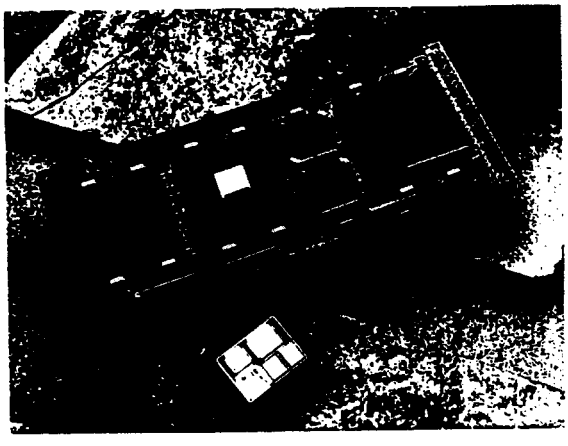
ROSS (SPARC) MODULE



- **5 VLSI components (0.8 micron) , comprising a complete central processor chipset**
- **Normally packaged on a 3.3" x 7.25" PCB with a 100-pin connector**
- **Multi-die package version packaged in a single 224-pin CQFP**
- **Size of substrate is 0.93 in x 1.19 in (21x smaller in area than PCB)**
- **Contains 5 die (4 unique):**
  - **292 x 330 mils, 196 pads**
  - **420 x 393 mils, 166 pads**
  - **421 x 445 mils, 244 pads**
  - **337 x 269 mils, 50 pads**
- **3 million transistors in total**

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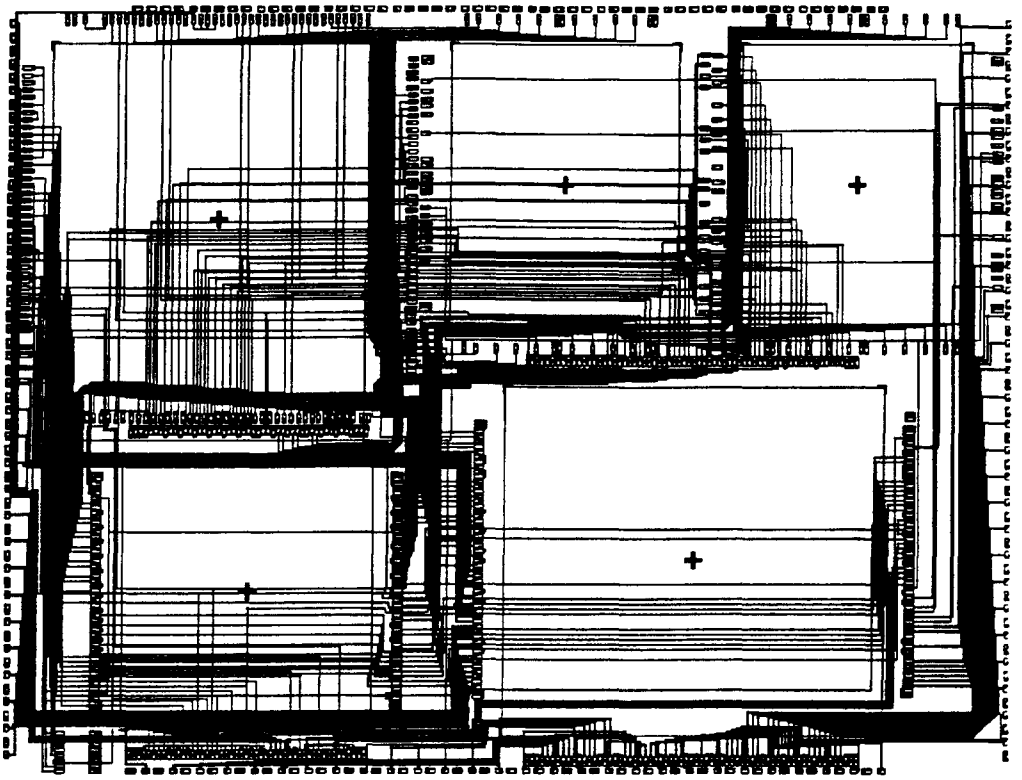
ROSS (SPARC) LAYOUT



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BENEFIT OF nCHIP TECHNOLOGY FOR ROSS APPLICATION

- Higher performance
  - All chip-to-chip delays are under 1 nsec
  - Clock skew between chips is less than 200 psec
  - Eliminates package-induced ground bounce and simultaneous switching noise
- Comparable in cost to single chip packaging approach with higher density

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SUMMARY

Single chip packaging solutions are becoming:

- More expensive due to increasing chip I/O
- More performance limiting due to increasing clock frequencies

nCHIP's MCM technology overcomes the limitations of single chip packaging solutions

- Supports high pin count ICs without cost or performance penalty
- Chip to chip delays are reduced to under 1 nsec
- Eliminates package-induced ground bounce