Introducing a Revolutionary 3 Dimensional Package Type

THE SLCC

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CIRCUIT DENSITY

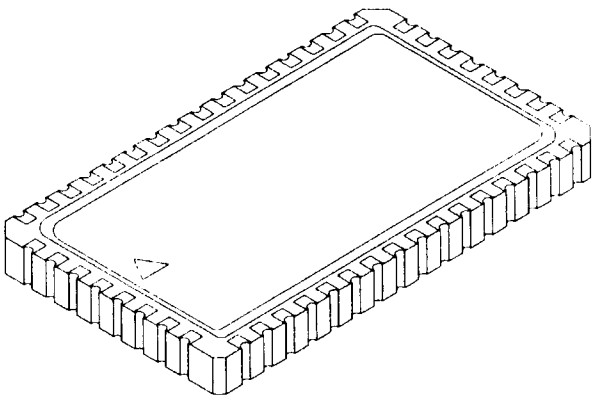
HIGHEST	STACK	Multi-chip Module using Stackable Leadless Chip Carriers (SLCC)
	DSMCM	Double Sided Multi-chip Modules
	HYBRID	Several Die in 1 Package
HIGHER	QFP	Quad Flatpack
	PGA	Pin Grid Array
	LCC	Leadless Chip Carrier
	PLCC	Plastic Leadless Chip Carrier
	SOJ	Small Outline Package
	SOIC	Small Outline I.C.
	FP	Flatpack
LOWER	DIP	Dual In Line Package

Multiple connections of the conventional type packages are done in a 2 dimensional plane.

Multiple connections of the Stackable Leadless Chip Carrier are done in 3 Dimensions, therefore a higher Circuit Density can be accomplished.

FEATURES OFF SLCC's

- Surface Mount technology
- Stackable Ceramic Leadless chip Carrier
- Hermetically Sealed
- Pinout Internally and/or Externally Configurable
- Operates over Full Military Temperature Range
- Typically Single I.C. *(Can Accept Multiple)*
- Can Easily Mirror Pinouts
- Small Size



SLCC CONSTRUCTION

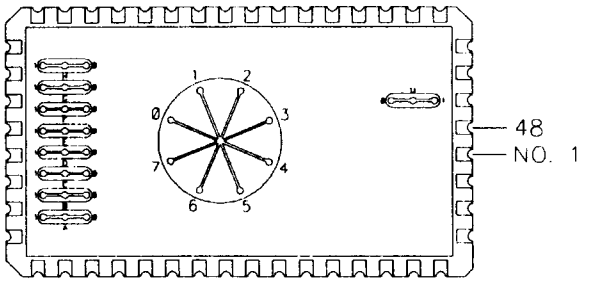


Figure 1.

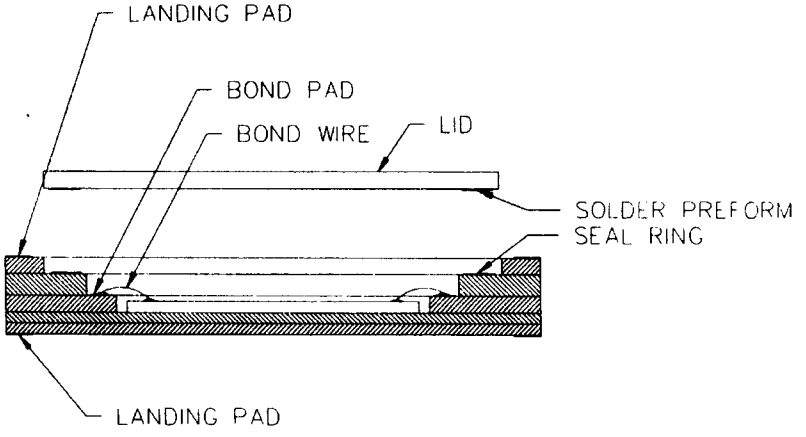
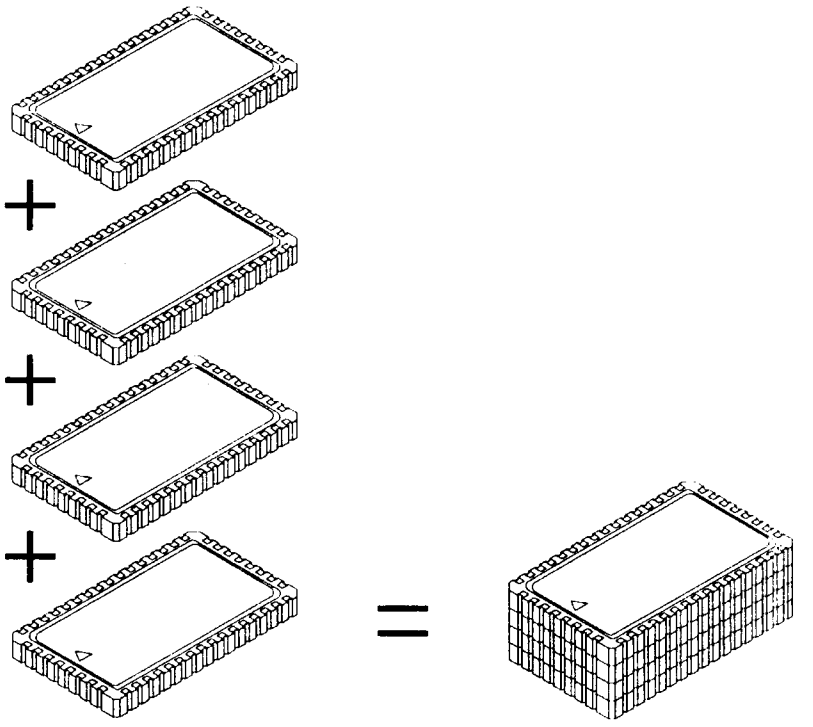


Figure 2.



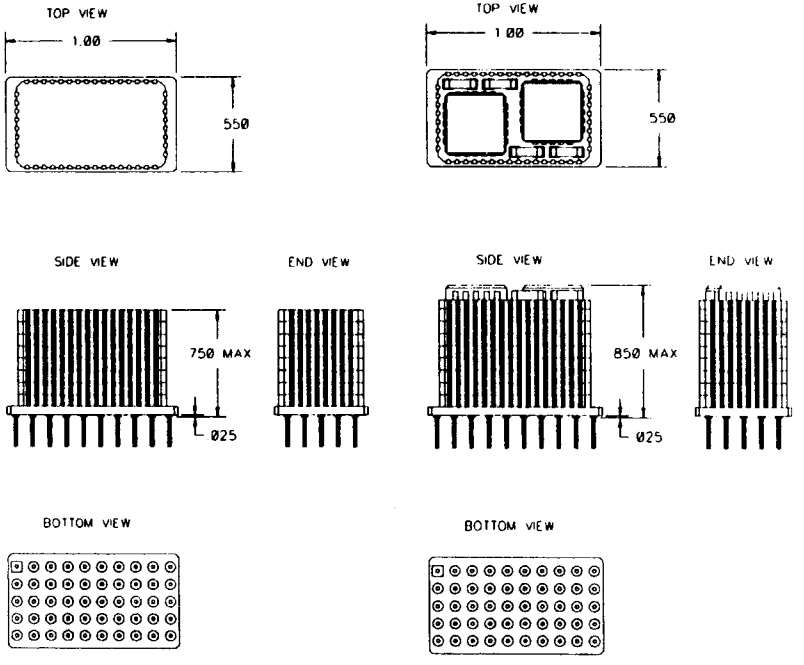
ANY NUMBER OF PACKAGES
CAN BE STACKED TO FORM A
LOGICAL CIRCUIT SUBSYSTEM.

APPLICATION 1

8-128K x 8 SRAM

(NOT DECODED OR BUFFERED)

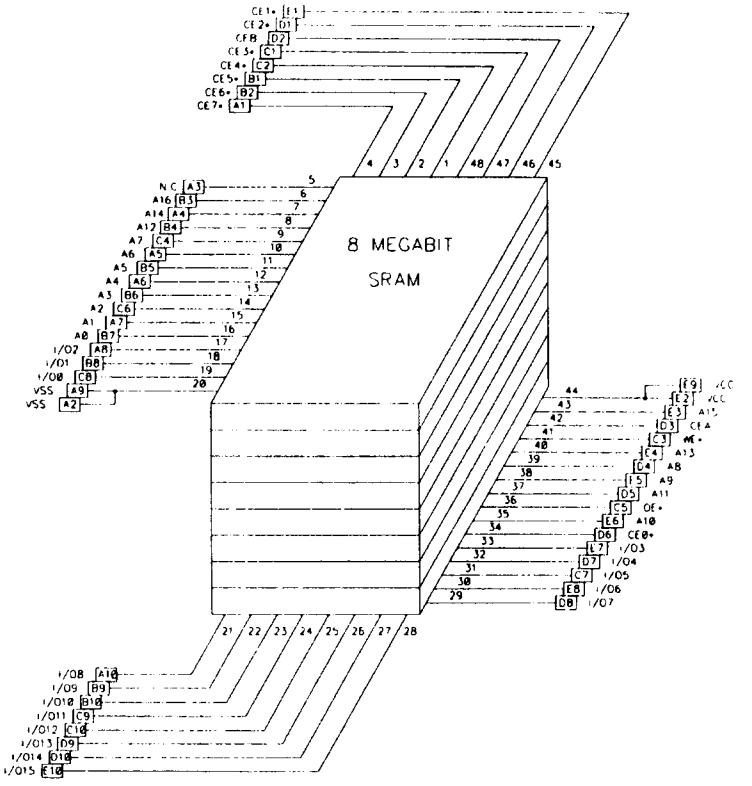
APPLICATION 2



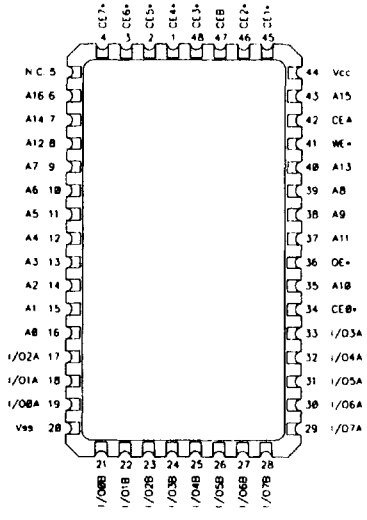
1MEG x 8 SRAM
or
512K x 16 SRAM

8 - 128K x 8 SRAM
1 - DECODER 139
1 - TRANSCIEVER

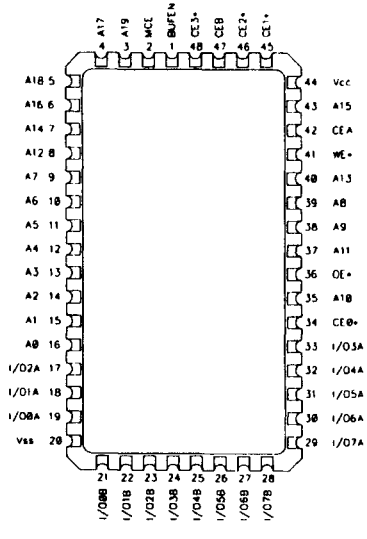
1MEG x 8 SRAM



CIRCUIT DIAGRAM



NOTES THIS SHOWS THE PINOUT ON THE STACK ALONE UP TO 16 SLCC IS POSSIBLE IN BY 8 MODE AND 32 SLCC IN BY 16 MODE



NOTES. THIS SHOWS THE PINOUT ON THE STACK WHEN IT IS DECODED AND BUFFERED

DENSE-STACK FEATURES

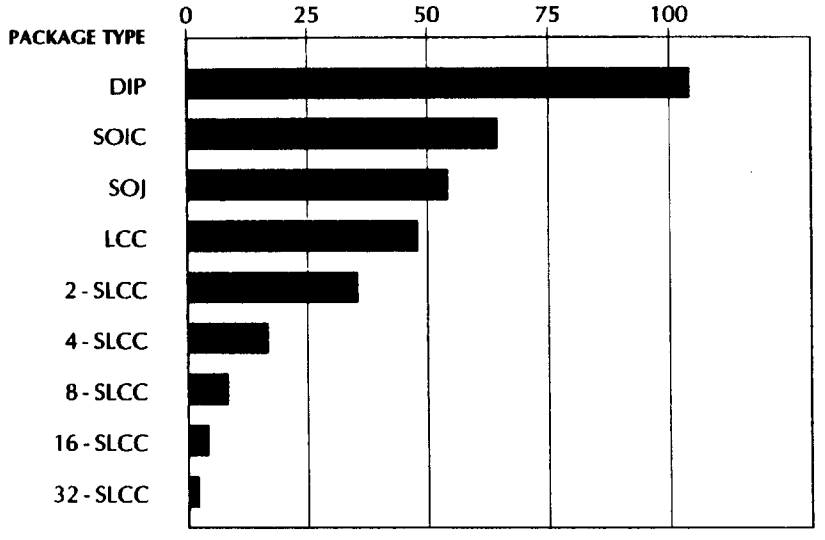
- Able to Parametricaly Test Components at Temperature Before Assembling Stack.
- Able to Environmentally Screen and Burn-In Components Before Assembling Stack.
- Able to Rework and Replace Bad Components After Stack has been Assembled.
- Able to Visually Inspect All Components After Assembling Stack (No Hidden/Buried Solder Connections).
- Able to Clean and Remove Flux Residue Because of Standoff Between Stacked Components.
- Better Electrical Performance Due to Extremely Short/Low Resistance Interconnects Between Components in Stack.

Circuit Board Features (Using Dense-Stack)

- Able to Upgrade or Revise Circuit Without Changing PWB Design.
- Increases Memory Density
    - Reduced Number of Layers
    - Reduced Number of Vias
    - Reduced Trace Lengths
    - Reduced Number of PWB's
- Operates over Full Military Temperature Range

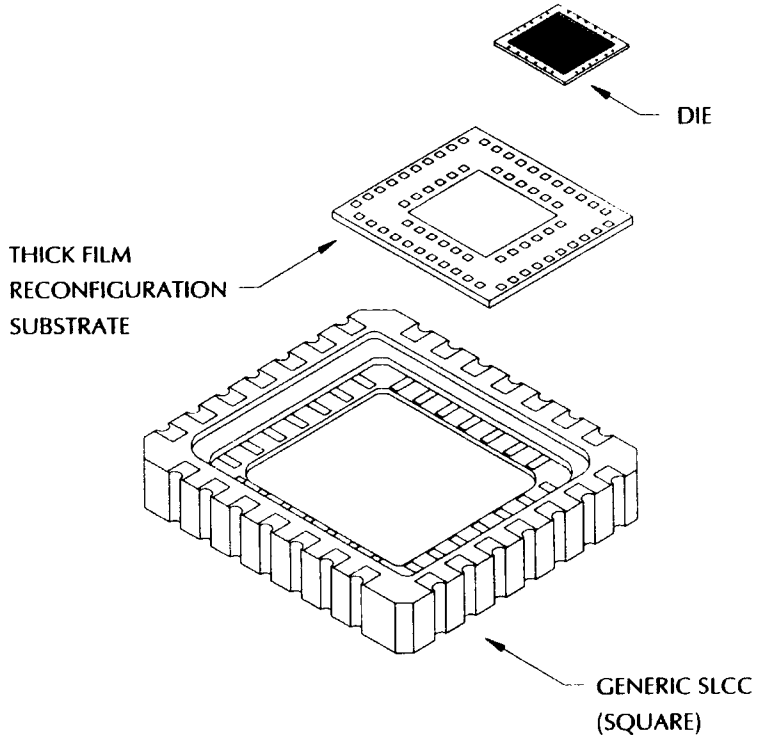
PCB AREA

(Square Inches)



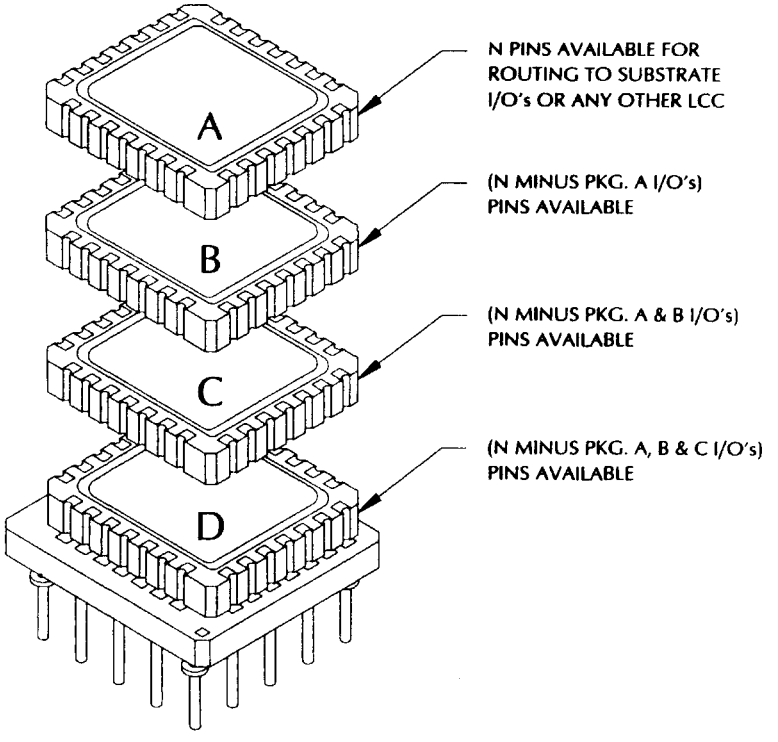
COMPARISON OF PCB SPACE REQUIRED FOR A 16 MEGABYTE SRAM SYSTEM FOR DIFFERENT PACKAGE TYPES.

GENERIC SLCC APPLICATION



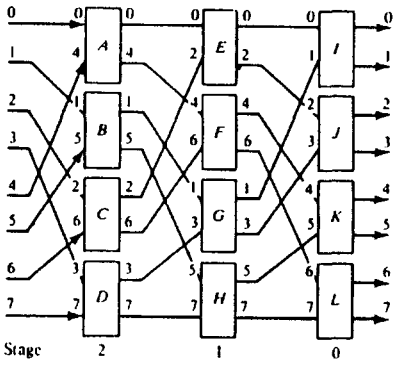
RECONFIGURATION SUBSTRATE ALLOWS ANY DIE CONFIGURATION OF N OR LESS BOND PADS TO BE CONFIGURED AT WILL TO THE LCC PINS.

AT THE STACK LEVEL



THE FEATURES NEEDED FOR A STACKABLE APPLICATION ARE CIRCUITS WITH SIMILAR DEVICES WITH HIGH NUMBER OF COMMON I/O AND PARALLELED CONTROL SIGNALS. EXAMPLES: MEMORY, MULTIPLEXERS, BUS INTERFACE, MULTIPROCESSORS.

SINGLE - INSTRUCTION - MULTIPLE - DATA MULTIPROCESSOR INTERCONNECTION SYSTEM



The shuffle-exchange network for $n = 8$ (Omega network)

FEATURES:

- 1.4" X 2.0" X 0.5" OUTER DIMENSIONS
- 160 PINS
- USES 48 - 157's (QUAD 2-INPUT MULTIPLEXERS)
- 8-BIT DATA PATH
- INDIVIDUAL SWITCHING BLOCK CONTROL PINS
- SAVE 256 PINS