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# R6000 Microprocessor
# RC6280 Compute Server

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## Outline

1. RC6280 System Overview
2. Technology
3. R6000 Chip Set
4. Cache Organization
5. Performance
6. Future Directions

# Design Goals

- Fastest complete system for $150,000
- Single-board processor
- Highly integrated VLSI chip set
- I/O and memory commensurate with processor
- Compatible with user-level R2000 instruction set



# RC6280 Performance / Expansibility

- 50 VUPS (VAX Units of Performance) @ 60 MHz
- 9 double precision Linpack megaflops (compiled)
- 240 megabytes/sec (peak) backplane bandwidth
- one to six VME busses
- 1 gigabyte main memory with 4 megabit chips

# RC6280 Architectural Features

- Two level cache
- 36-bit physical address
- R2000 instruction set with enhancements
  - Load/Store double floating-point
  - Synchronization (load-locked, store-conditional)



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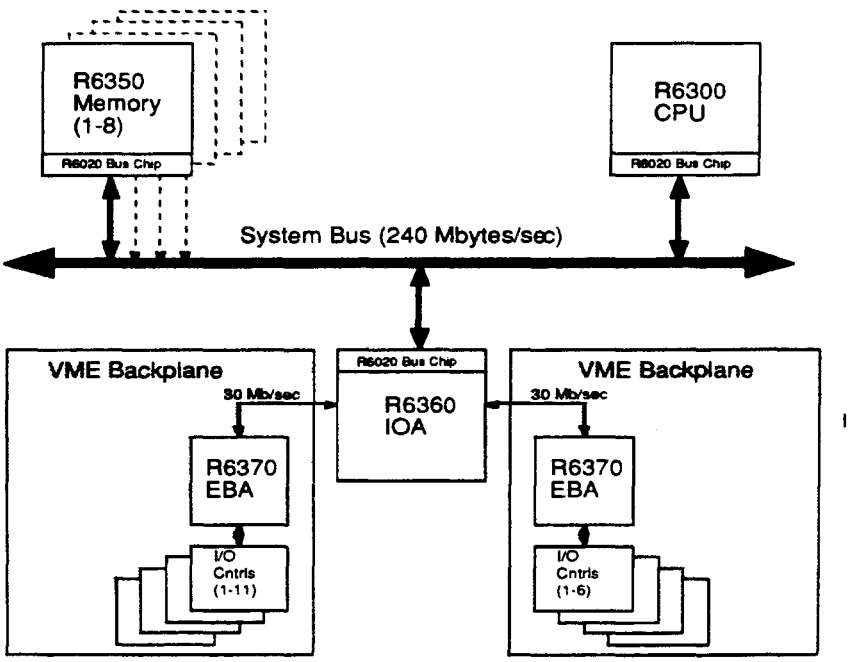
## RC6280 System Block Diagram



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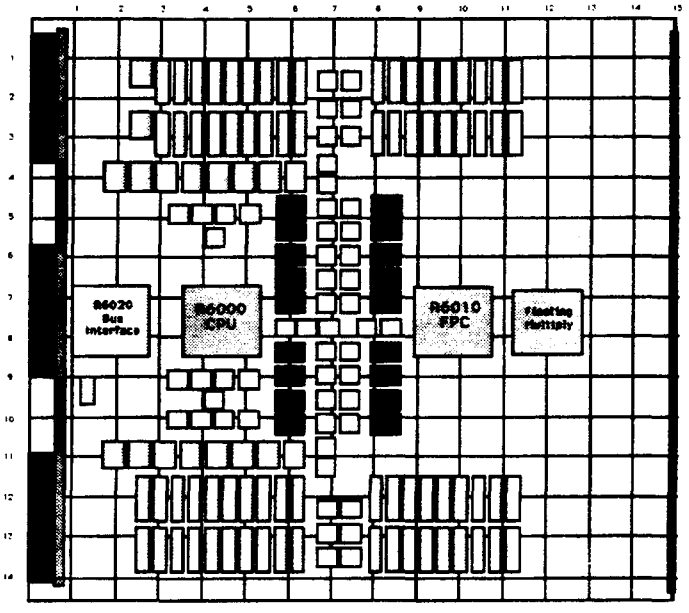
## CPU Board Placement



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# Technology Overview

- ECL VLSI using standard cell design methodology
- Small, fast ECL gate arrays for VLSI to cache interconnect
- 8 ns 4Kx4 and 16Kx4 primary cache RAMs (ECL, BiCMOS)
- 15 ns 64Kx1 secondary cache RAMs (BiCMOS)

- All components designed for air-cooling at 400 LFM (45° C rise)
- VLSI devices packaged in 259-pin ceramic PGAs
- 100K temperature compensated signal levels
- Buried termination resistors to reduce stubs at PGAs



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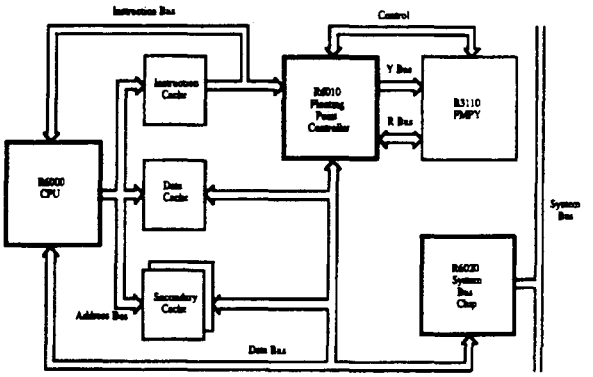
# R6000 Chip Set

- four VLSI chips -- CPU, FPC, FMPY, Bus
- tightly coupled CPU/FPC interface
- system bus completely defined by Bus chip
- on-chip address translation and cache control





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# R6000 Chip Set Physical Parameters

| | *R6000 CPU* | *R6010 FPC* | *R6020 Bus* |
|---|---|---|---|
| die size (mm) | 9.9x10.1 | 9.9x9.6 | 9.4x9.6 |
| power | 23W | 20W | 20W |
| transistor count | 89K | 88K | 91K |
| resistor count | 54K | 54K | 66K |
| number of cells | 4468 | 4238 | 4002 |
| signal pins | 184 | 173 | 155 |
| package pins | 259 | 259 | 259 |



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# Cache Organization

- two-level cache (64K I, 16K D, 512K Secondary)
- separate primary caches, combined secondary cache
- virtually indexed primary, physically indexed secondary
- virtual tags on both caches
- on-chip TLB slice, in-cache full TLB
- entire design requires only six banks of RAM



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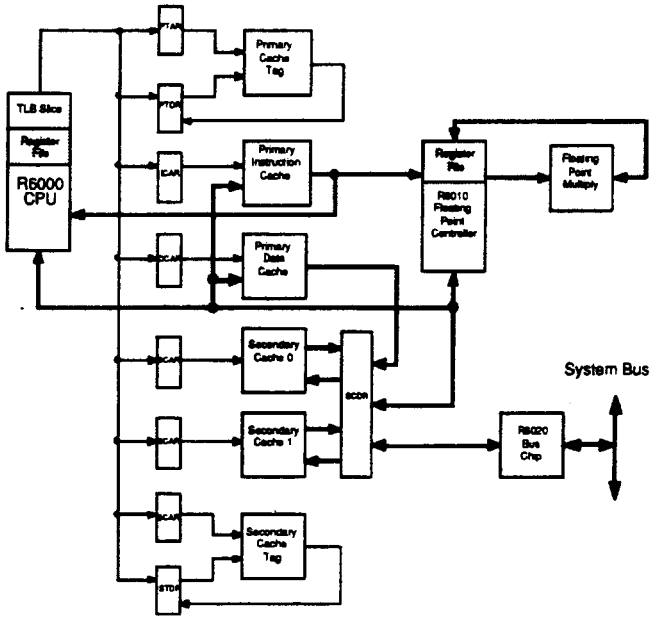
# Processor Block Diagram



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# Primary Caches

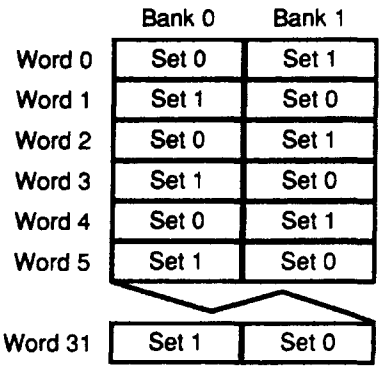
- Primary instruction cache
  - direct mapped
  - 8-word line size
  - refill -- 10 cycles and restart
- Primary data cache
  - write-through
  - 2-word line size
  - refill -- 1 cycle and restart
- Virtual addresses and virtual tags (including PID)
- Shared tag -- pretest mechanism



# Secondary Cache

- 512 Kbytes - 2 Megabytes
- two-way set associative
- physical addresses, virtual tags (including PID)
- 32-word line size
- write-back
- two cycle access to each side
- ping-pong for block transfers at one word per cycle
- refill -- 65 to 80 cycles

# Secondary Cache Lines



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# Address Translation

- no translation to primary caches
- physical index to secondary cache is simpler for OS
- 6-bit wideTLB slices in CPU-- separate instruction and data
- TLB and physical tags held in reserved portion of secondary cache
- full-width TLB read only after secondary cache miss



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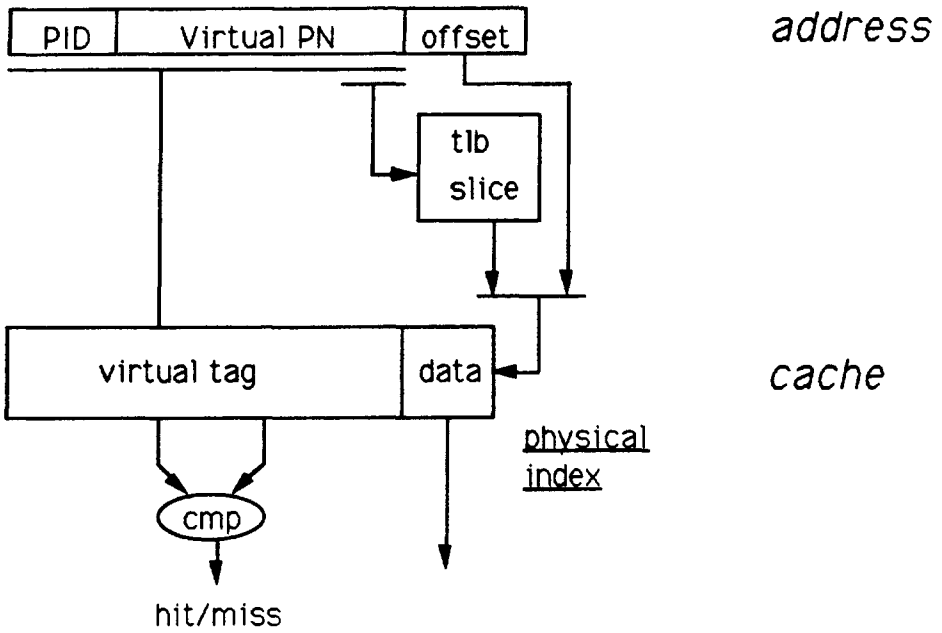
PID
Virtual PN
offset
address
tlb
slice
virtual tag
data
cache
physical
index
cmp
hit/miss



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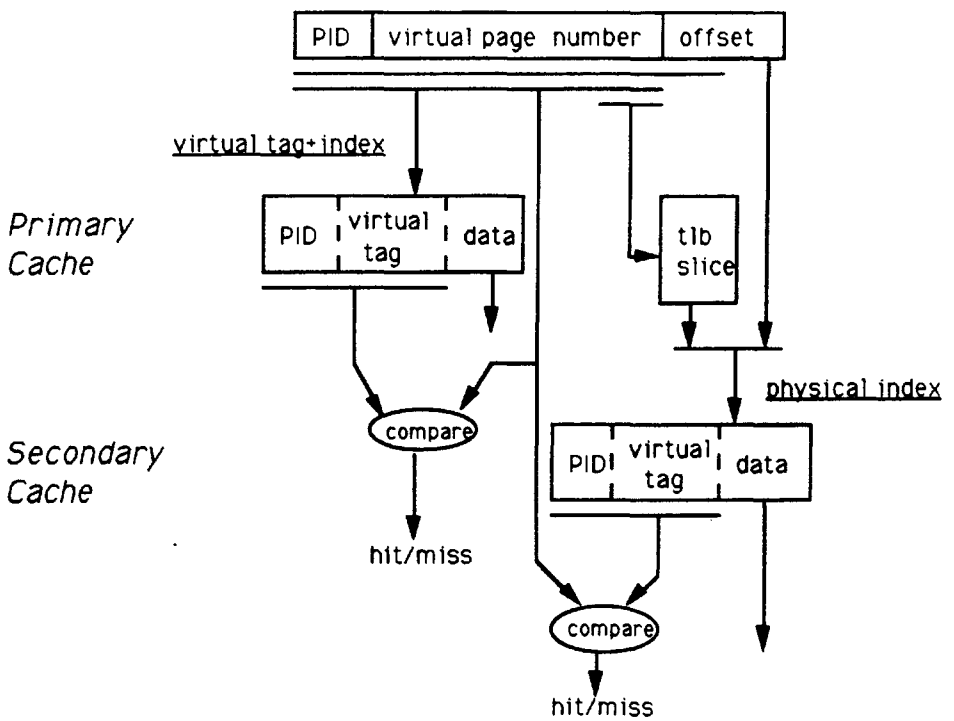
PID
virtual page number
offset
virtual tag+index
Primary
Cache
PID
virtual
tag
data
tlb
slice
physical index
compare
Secondary
Cache
PID
virtual
tag
data
hit/miss
compare
hit/miss



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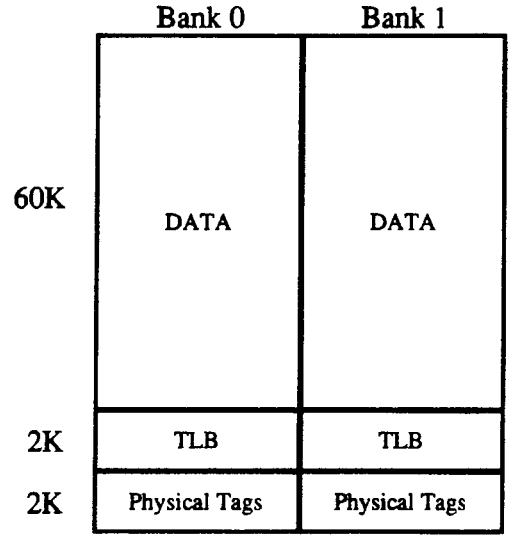
# Secondary Cache Organization



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# Secondary Cache Miss Sequence

- detect virtual miss
- read TLB entry
- check for TLB miss
- check for TLB slice miss
- read physical tags -- compare with TLB entry to detect physical hit



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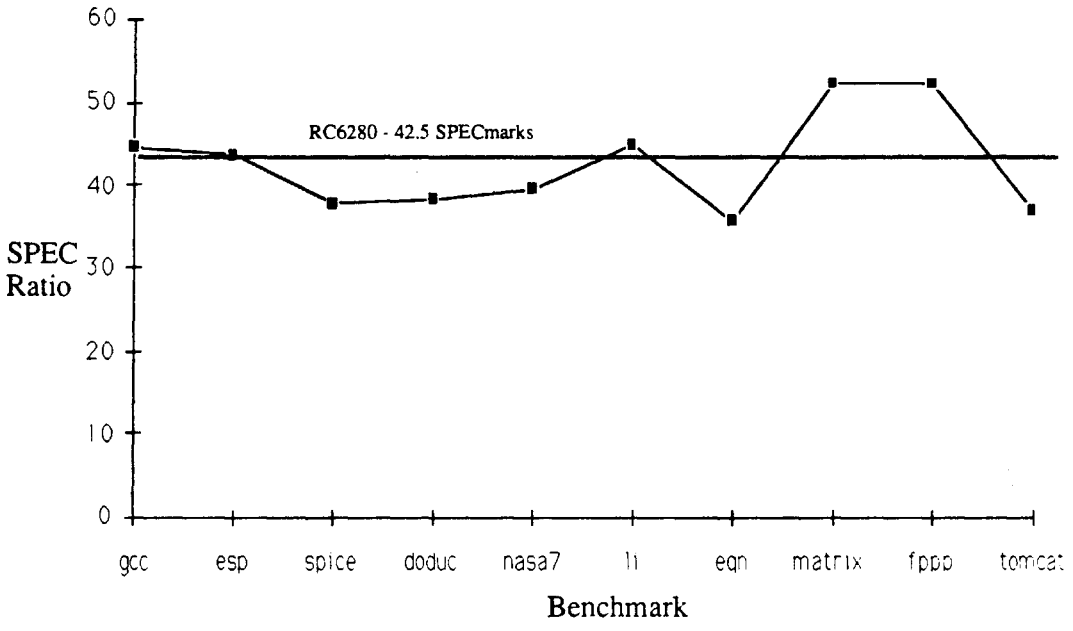
# RC6280 Performance:
## SPEC Rating - 42.5 SPECmarks

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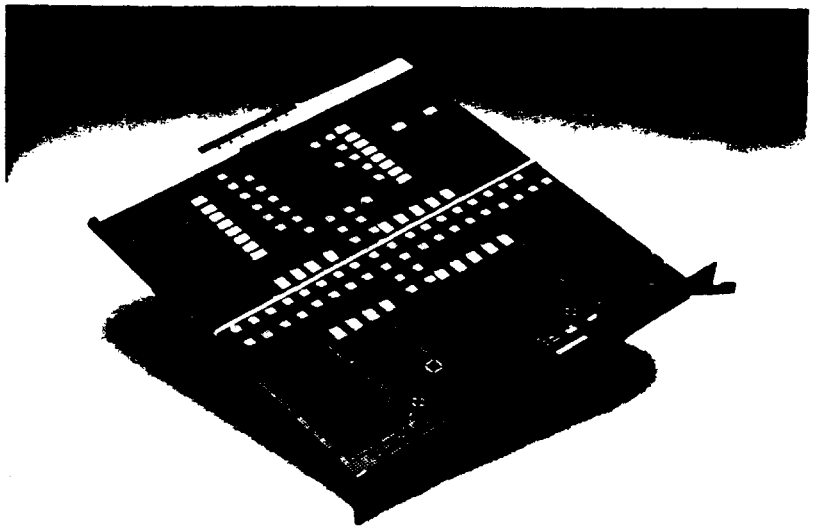

# Future Directions

- Faster transistors
- Smaller metal and via pitches
- More layers of metal
- Lower capacitance
- Multiple voltages (GND, -5, -2)
- Higher power

Single chip CPU/FPU

Wider data paths to cache

Highly integrated caches

Deeper pipeline

Multiple instruction issue