HOT CHIPS II

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The SPARC Lightning Processor

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Lightning Project

A Superscalar+ SPARC Microprocessor

- Based on Metaflow architecture from Metaflow Technologies, Inc. of San Diego, CA.
- Joint development of Metaflow, LSI Logic, Hyundai Electronics.
- SPARC CMOS processor chipset packaged as Sun Mbus-2 "module".
- Estimated performance: Average 100 MIPS with 50 MHz clock (from a peak rate of 200 MIPS).
- Samples scheduled for Q2 1991

Distinguishing Features of SPARC Lightning Processor

Metaflow Superscalar+ Architecture

- Four instructions issued per clock (up to 3 integer/floating point instructions and one branch).
- Six parallel functional units (3 integer ALUs, two floating point ALUs, 1 branch unit).
- Dataflow-based out-of-order instruction issue/execution (both memory and ALU operations), in-order completion, with precise traps and interrupts.
- Speculative execution beyond unresolved conditional branch instructions (through multiple basic blocks, with instant state repair on error).
- Above mechanisms are completely transparent to executing program (strict SPARC ABI compatibility).

Lies, Damn Lies, and Benchmarks

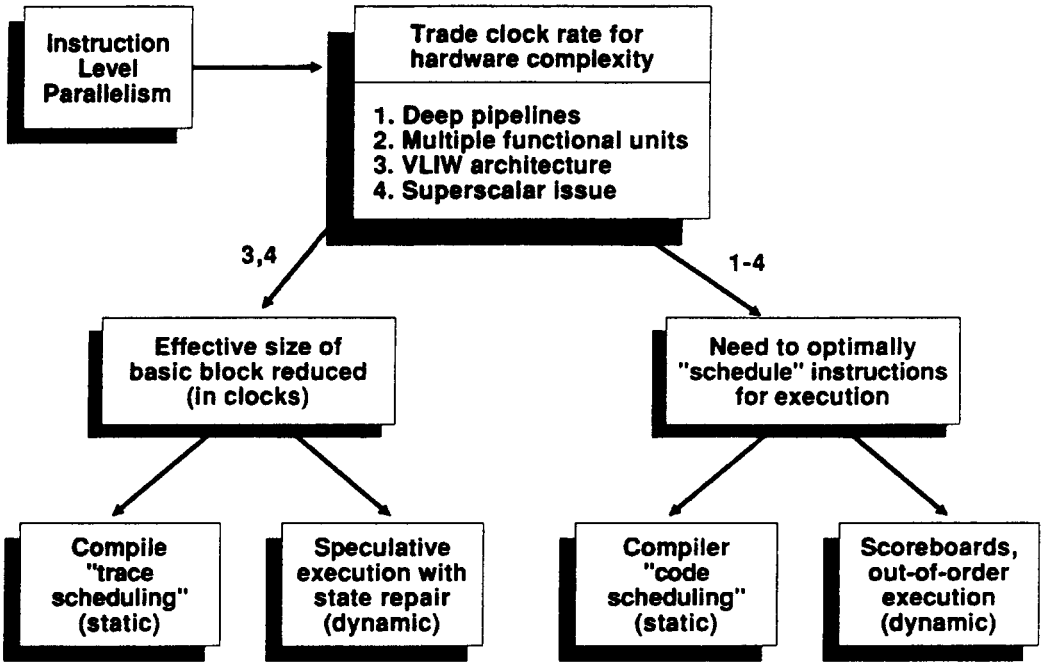
Benchmark	IPC	MIPS	MFLOPS	Remarks
Dhrystone (ver 1.1)	2.3	>110	n/a	
SPECmark (integer)				
gcc	*	*	n/a	
espresso	*	*	n/a	
li	*	*	n/a	
eqntott	*	*	n/a	
SPECmark (FP)				
spice	*	*	*	
doduc	*	*	*	
nasa7	*	*	*	
m300	*	*	*	
fpppp	*	*	*	
tomcatv	*	*	*	

* To be supplied at conference.

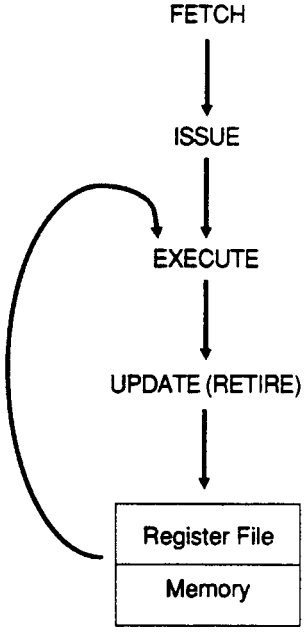
Notes:

1. Based on RTL-level simulations of processor, caches, Mbus and DRAM memory, 50 MHz processor clock, compiled using unmodified Sun SPARC compilers.
2. IPC = instructions per clock, MIPS = millions of SPARC instructions per second, MFLOPS = millions of floating point operations per second.

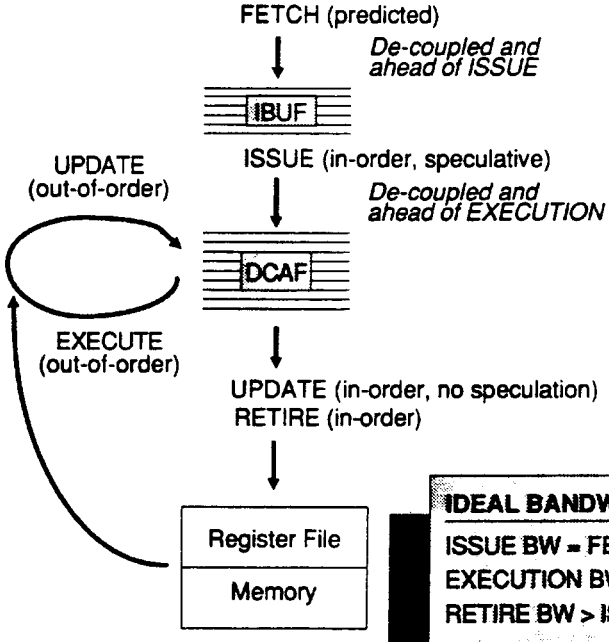
INSTRUCTION-LEVEL PARALLELISM DESIGN TRADEOFFS



IN-ORDER PIPELINE



METAFLOW PIPELINE

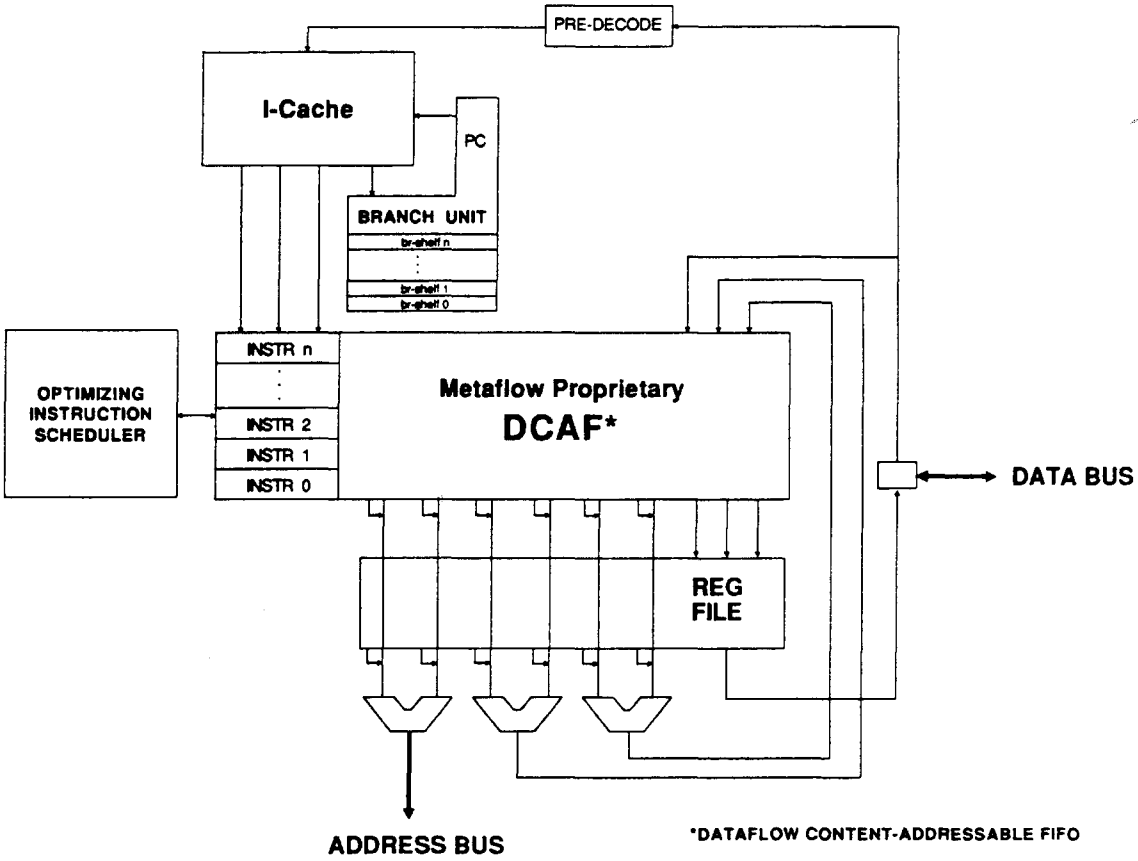


IDEAL BANDWIDTH (BW):

ISSUE BW = FETCH BW
EXECUTION BW > ISSUE BW
RETIRE BW > ISSUE BW

LIGHTNING:

ISSUE/FETCH BW = 4 instr
EXECUTION BW = 6 instr
RETIRE BW = 7 instr



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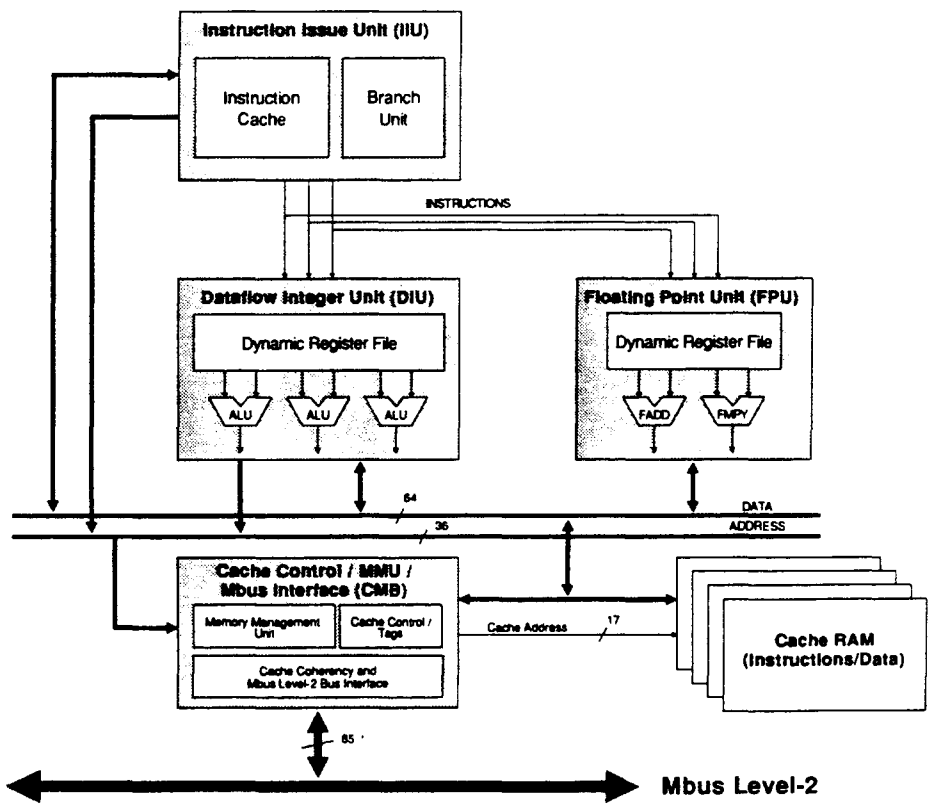
Lightning SPARC Mbus Module



Observations Regarding the SPARC Lightning Processor

- Sustained execution with IPC ≈2 common
- Out-of-order issue/execution key to good performance
- Processor constantly "in speculation" (typical basic block is <2 clocks!)
- Relative insensitivity to memory latency for data (due to DCAF)
- Optimal "code scheduling" by compiler **not** important
- "Delayed instruction" after branch a nuisance (1 delayed instruction ≡ 1/4 "extra" clock)
- Fundamental limits to performance:
  - Memory port bandwidth (single 64-bit port)
  - Branch prediction rate (unwanted speculative execution)
  - Calculated branch address latency (e.g., "jump tables")
  - Instruction cache hit rate