SPEC

GaAs SPARC™ RISC Processor

Developed by
Systems & Processes Engineering Corporation (SPEC)
1406 Smith Road, Austin, Texas 78721

Program Sponsored by
National Aeronautics and Space Administration (NASA)
Goddard Space Flight Center (GSFC)

Presented by
Gary McMillian, Ph.D.

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SPEC

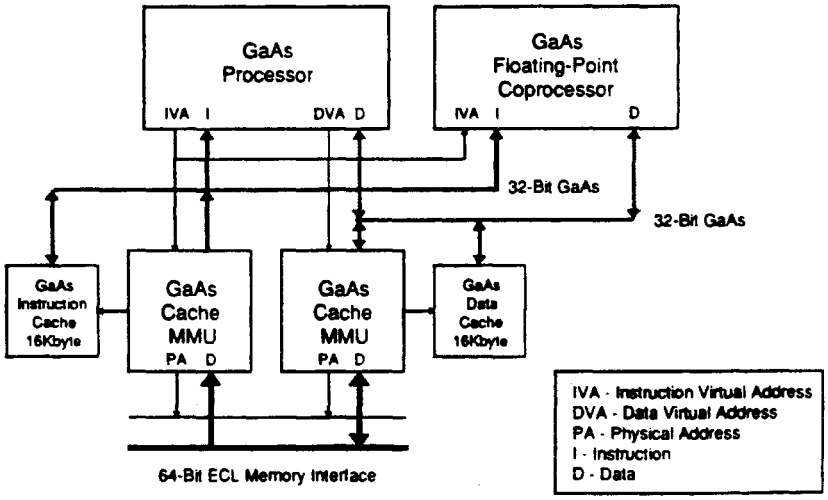
SPARC Architecture

- Sun Microsystems' Scalable Processor ARChitecture (SPARC™)
- RISC Architecture with Fixed Length 32-bit Instructions
- Large "Windowed" Register File (2 - 32 Windows)
- Memory Access with Load and Store Instructions
- Delayed Control Transfer (e.g. Delayed Branch Instruction)
- Tagged Arithmetic Functions to Support AI Operations
- Compatible with DARPA's RISC Core Instruction Set Architecture

GaAs SPARC Performance

- Design Goal - 200 MHz Clock Frequency » 5 nsec Clock Cycle
- 4 Stage Pipeline » Effectively 1 Instruction per Clock Cycle
- Most Instructions Execute in 1 Cycle » 200 MIPS Peak
- Minimum of 6 Register Windows » 104 32-Bit Registers
- Designed for Vitesse Semiconductor's DCFL GaAs Process

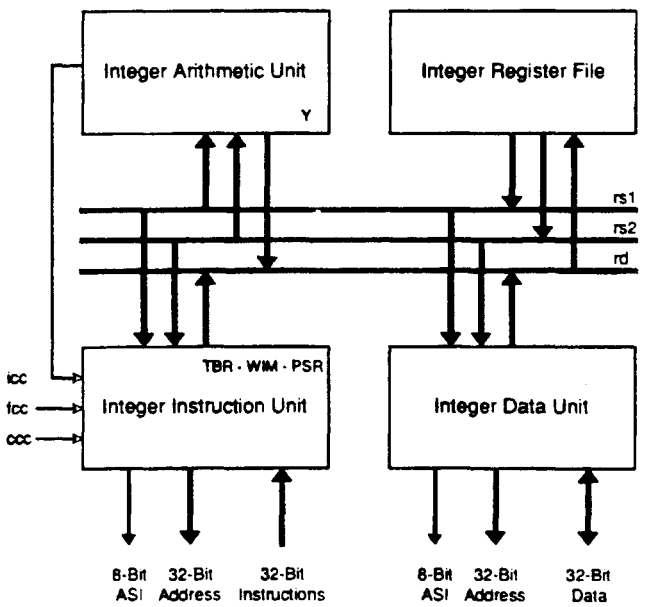
GaAs SPARC Processor



GaAs SPARC Integer Unit

- Harvard Architecture
  - 32-Bit Instruction Bus
  - 32-Bit Data Bus
- Parallel Execution Units
  - Integer Instruction Unit
  - Integer Data Unit
  - Integer Arithmetic Unit
- Pipelined Design
  - Address - Decode - Execute - Writeback Pipeline

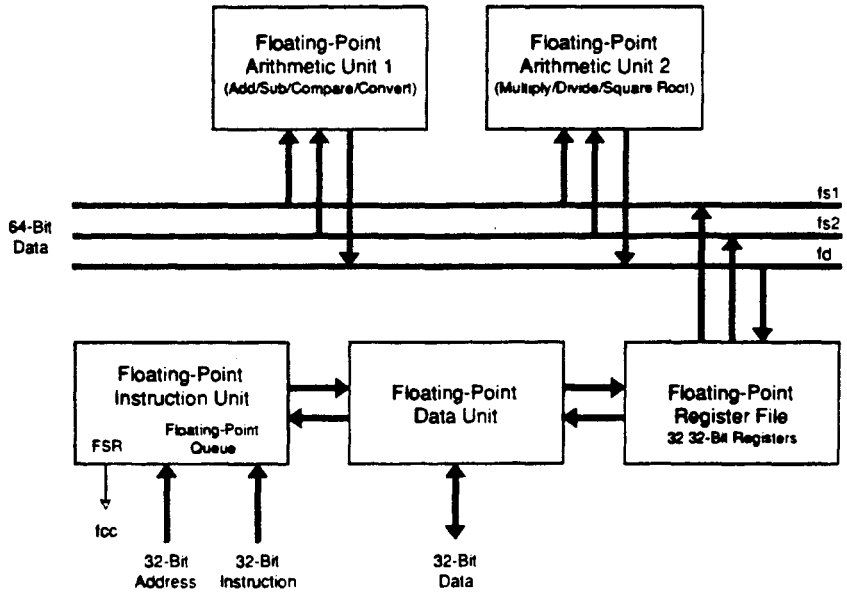
GaAs SPARC Integer Unit



GaAs SPARC Floating Point Unit

- Coprocessor Interface to GaAs RISC Processor
- Single and Double Precision Floating Point Operations
- SPARC - IEEE 754 Compliant
- Two Parallel and Pipelined Floating Point Units
  - Add, Subtract, Compare, Convert
  - Multiply, Divide, Square Root
- 64-Bit Internal Data Bus
- Multiple Entry Instruction Queue

GaAs SPARC Floating Point Unit

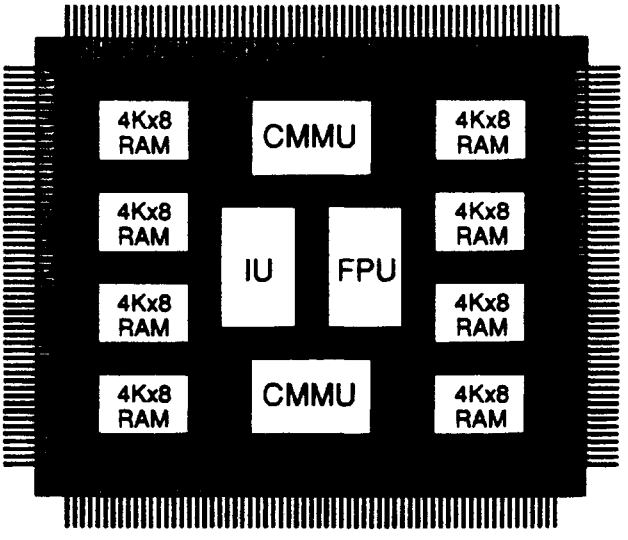


GaAs SPARC CMMU

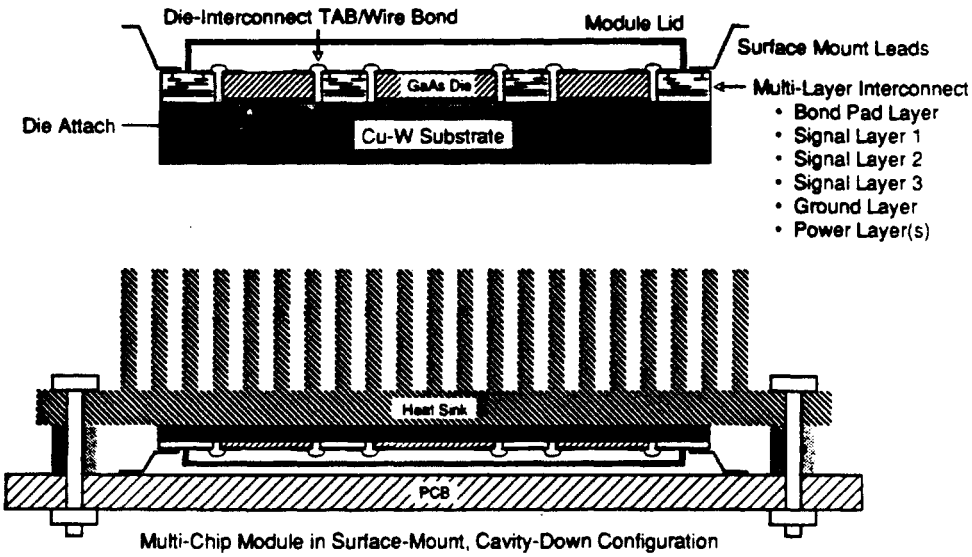
- Direct Map Virtual Cache
- 512 Cache Tag Entries with a 32 byte Cache Line Size
- 16K byte GaAs Cache Memory (4Kx8 GaAs RAM, 2.5 nsec Access)

- MMU Designed to SPARC Reference MMU Specification
- 4G byte Virtual Address Space
- 64G byte Physical Address Space
- 4K byte Page Size
- Context Table plus 3 Levels of Page Tables (Page Table Pointers)
- Page Table Entry (PTE) Descriptors Provide Virtual-Physical Mapping
  - Physical Page Number, Access Permission
  - Cacheable, Modified, Referenced
- Page Descriptor Cache of PTEs

GaAs SPARC Multi-Chip Module



GaAs SPARC Multi-Chip Module



Multi-Chip Module in Surface-Mount, Cavity-Down Configuration