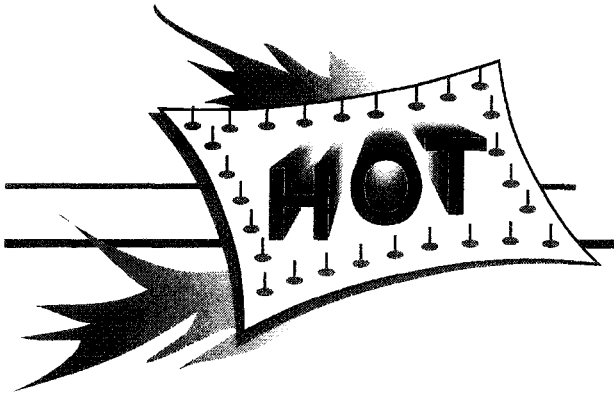

Hot Chips Symposium

Santa Clara University
Santa Clara, California
Monday & Tuesday, August 20-21, 1990

Symposium Record

Sponsored by the Technical Committee on Microprocessors and Microcomputers of the IEEE COMPUTER SOCIETY

Chips Symposium II

Santa Clara University, Santa Clara, California
Monday & Tuesday, August 20 - 21, 1990

It is my pleasure to welcome you to the second **Hot Chips Symposium**. Last year, through the initiative of Dr. Robert Stewart and Professor Glen Langdon as members of the **Technical Committee on Microprocessors and Microcomputers** of the IEEE Computer Society, the first Hot Chips Symposium was organized and held in May at Stanford University. The goal of the symposium was to provide a forum to present the latest high performance chips used to build high performance workstations and systems. The Symposium was extremely well received.

This year's symposium follows the footsteps of last year's symposium and expands its scope slightly to include broader issues, such as performance, software, and interconnects. This year's program features a banquet on the first evening, with a distinguished guest speaker from the venture capital community, Mr. John Doerr. Mr. Doerr is a General Partner with Kleiner Perkins Caufield and Byers. He also serves on the Board of Directors for Sun Microsystems and Cypress. We all look forward to hearing an interesting presentation on the direction of high performance chips and the views of the venture capital community about it.

I would like to express my gratitude to a number of people who made this year's symposium possible. First I would like to thank the two Program Co-Chairmen Alan J. Smith and John Crawford who have managed to put together through the efforts of their Program Committee an excellent technical program. I would also like to thank the members of the Organizing Committee, Doug Marquardt for the many hours he has spent in planning and setting up the local arrangements, Stacy Peña and Andy Goforth for the meticulous and hard work they have put in pulling together the publicity for this symposium, Nam Ling for keeping the process of registering the large number af attendees under control with the little secretarial help he's got, Cynthia Wirtz for planning and working out the details for putting together the Digest of Presentations, Bob Stewart for handling the treasury and volunteering to help in resolving so many other unimaginable details for organizing this symposium, Martin Freeman for his valuable advice, and Glen Langdon, the TCMM Chairman, for passing his experience along to the new members of the Organizing Committee.

I wish you a good time at Hot Chips II.

Sincerely yours,

Hasan S. AlKhatib
General Chairman

HOT CHIPS II: A Symposium on High Performance Chips

FOREWORD

The most exciting frontier in the computer and electronic industries is the development of powerful single chip (or chipset) processors of various types. Only recently has it become possible to put mainframe levels of computing on single chips, and to place on a desk a level of computing performance that exceeds what was available in even the largest computer centers 15 years ago. This conference was first offered last year in order to provide a forum for the presentation of up-to-the-minute, state-of-the-art presentations about the most exciting developments in the chip and chip-set world - i.e. "hot chips". The enormous response in 1989, of about 500 attendees, confirms the excitement that many of us feel about current developments.

This year, we received about 50 submissions and selected the 26 that we found most interesting. We would like to have accepted more, but squeezing even the existing program into two days has been a challenge; we dropped plans for keynote speakers and panel sessions in order to accommodate interesting product talks. We also made an effort to broaden the coverage of the conference, and we are happy to note the presence of sessions and talks on topics such as packaging, routing, systolic and array processors, video and data compression processors, and benchmarking, in addition to the usual coverage of high performance microprocessors and floating point and DSP chips. Many of the submittals were accompanied with notes indicating that the material was confidential until the conference; some of the presentations are the first public discussions of those products. We have been disappointed that we weren't able to attract more submissions from outside the United States; we hope that this conference will have more of an international component in the future. We urge those of you reading this foreword to consider proposing a talk when the call for proposals appears next year.

Many of the presenters at this conference will be asked to prepare papers for consideration by IEEE MICRO, and those papers selected will appear in the Spring of 1991.

We'd like to thank the conference organizing committee for setting everything up, making local arrangements, doing publicity, publishing the program, paying the bills, doing registration, reminding the program committee that it was time to create a program, and performing many other tasks that we don't even want to think about. We'd also like to thank the members of the program committee for their efforts in attracting and soliciting a good set of proposals, and in working with the presenters to ensure high quality presentations of substantial technical content.

Alan Jay Smith
John Crawford
Program Co-Chairs

MONDAY

August 20, 1990 – Mayer Theater, Santa Clara University

On-site registration 8:00 - 9:00 am

9:00–9:30 **Welcome and Opening Remarks**
Hasan Alkhatib, General Chair
Alan Jay Smith and John Crawford, Program Co-Chairs

9:30–11:00 **High Performance Processors – I** Session Chair: David Ditzel

- **GaAs SPARC RISC Processor**
  Gary McMillian, Systems & Processes Engineering Corp., Austin, TX
- **The SPARC Lighting Processor**
  Bruce Lightner, Metaflow Technologies, San Diego, CA
- **The MIPS R/6000 Microprocessor**
  George Taylor, MIPS Corporation, Sunnyvale, CA

11:00–11:30 **Coffee Break**

11:30–12:30 **Performance** Session Chair: Alan Jay Smith

- **The SPEC and Perfect Club Benchmarks: Promises & Limitations**
  Rafael Saavedra-Barrera, University of California, Berkeley
- **Performance Characteristics of the I960CA Superscalar Microprocessor**
  Steven McGeady, Intel Corporation, Santa Clara, CA

12:30–2:00 **Lunch**

2:00–2:30 **Special Memorial Presentation on Dr. Robert Noyce**
Dr. Gordon Moore, Chairman of the Board, Intel Corp., Santa Clara, CA

2:45–4:15 **Video and Graphics** Session Chair: Hasan Alkhatib

- **A Video Compression Chip Set**
  Peter Ruetz, LSI Logic Corp., Milpitas, CA
- **C_Cube CL550 Image Coprocessor**
  Steven Purcell, C_Cube Corporation, San Jose, CA
- **DVI and 1750 Chip Set**
  Sanjay Vinekar, Intel Corporation, Princeton, NJ

4:15–4:45 **Soda Break**

4:45–5:45 **Packaging** Session Chair: Theresa Meng

- **Dense Stack**
  John Forthun, Dense-Pac Microsystems, Inc., Garden Grove, CA
- **Silicon Multichip Modules**
  Donald Benson, nChip Inc., San Jose, CA

5:50–6:50 **Floating Point** Session Chair: Theresa Meng

- **A 120 MFLOP CMOS Floating Point Unit**
  Alan Quek, Weitek Corporation, San Jose, CA
- **A 100MHz Floating Point/Integer Processor**
  Gregory Taylor, Bipolar Integrated Technology, Inc., Beaverton, OR

7:30 **Banquet with Speaker John Doerr,** General Partner with Kleiner Perkins Caufield & Byers

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Organizing Committee for the HOT Chips Symposium II:

Hasan Alkhatib, General Chair, Santa Clara University

John Crawford, Program
Intel Corporation

Alan Jay Smith, Program
U. C. Berkeley

Robert Stewart, Treasurer,
Past General Chair
Stewart Research Enterprises

Nam Ling, Registration
Santa Clara University

Doug Marquardt, Local
Arrangements, Santa Clara Univ.

Cynthia Wirtz, Publications
CrossCheck Technology

Martin Freeman, TCMM Member
Philips Research Center

Andy Goforth, Publicity
NASA Ames Research Center

Glen Langdon, TCMM Chair &
Publicity, U. C. Santa Cruz

Stacy Peña, Publicity
CrossCheck Technology

Jack Grimes, Past Prog. Co-Chair
Mass Microsystems

TUESDAY

August 21, 1990 – Mayer Theater, Santa Clara University

On-site registration 8:00 – 8:45 a. m.

8:45–10:45 **High Performance Microprocessors - II**
Session Chair: Martin Freeman

- **96-bit General Purpose IEEE 754 Floating Point Dual Port Processor**
  Terry Schultz, Motorola, Anaheim, CA
- **A Single Chip Integer VLIW Processor Core**
  Gerrit Slavenburg, Philips Research, Sunnyvale, CA
- **The Clipper Super Scalar CMOS Chip Set**
  Howard Sachs, Integraph Corporation, Palo Alto, CA
- **Experience with the i860 CPU**
  John Casey, Hauppauge Corporation, Hauppauge, NY

10:45–11:15 **Coffee Break**

11:15–12:45 **Systolic and Arrays** Session Chair: John Crawford

- **The Touchstone DELTA Prototype: A 30 Gigaflop Scalable Parallel Computer**
  Justin Rattner and others, Intel Corporation, Aloha, OR
- **100 MOP LIW Microprocessor for Multicomputers**
  Craig Peterson, iWarp Group, Intel Corporation, Aloha, OR
- **DataWave - a Data Driven Video Signal Array Processor**
  Ulrich Schmidt, ITT Intermetall, Freiburg, Germany

12:45–2:15 **Lunch**

2:15–3:45 **Routing and Interconnect** Session Chair: Forest Baskett

- **Caltech Mesh-Routing Chips**
  Charles Seitz, California Institute of Technology, Pasadena, CA
- **Get Off the Bus and Call a Taxi**
  Paul Scott, Advanced Micro Devices, Sunnyvale, CA
- **Hot Rod: 1Gbit/sec. Data Communications**
  Johnathan Zierk, Gazelle Microcircuits, Inc., Santa Clara, CA

3:45–4:15 **Soda Break**

4:15–5:45 **IBM's New Superscalar RISC** Session Chair: David Patterson

- **RISC System/6000 Architecture, Implementation, and Performance**
  B. Bakoglu and R. Oehler, IBM Watson Res. Ctr., Yorktown Heights, NY
- **Compiling for the RISC System/6000 Branch Unit**
  Martin Hopkins, IBM Watson Research Ctr., Yorktown Heights, NY
- **RISC System/6000 Floating Point Unit**
  Troy N. Hicks, Oscar R. Mitchell, and Richard E. Fry, IBM Advanced Workstation Div., Austin, TX

5:45 **Closing Remarks**

Program Committee for the HOT Chips Symposium II:

Alan Jay Smith and John Crawford, Program Co-Chairs

Forest Baskett Silicon Graphics Computer Sys.	**John Hennessy** Stanford University	**David Patterson** U. C. Berkeley
David Ditzel Sun Microsystems	**Teresa Meng** Stanford University	**Mario Tokoro** Keio University, Japan