

August 20, 1990 – Mayer Theater, Santa Clara University

On-site registration 8:00 - 9:00 am

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9:00–9:30 Welcome and Opening Remarks

Hasan Alkhatib, General Chair
Alan Jay Smith and John Crawford, Program Co-Chairs

9:30–11:00 High Performance Processors – I Session Chair: David Ditzel

- **GaAs SPARC RISC Processor**
Gary McMillian, Systems & Processes Engineering Corp., Austin, TX
- **The SPARC Lighting Processor**
Bruce Lightner, Metaflow Technologies, San Diego, CA
- **The MIPS R/6000 Microprocessor**
George Taylor, MIPS Corporation, Sunnyvale, CA

11:00–11:30 Coffee Break

11:30–12:30 Performance Session Chair: Alan Jay Smith

- **The SPEC and Perfect Club Benchmarks: Promises & Limitations**
Rafael Saavedra-Barrera, University of California, Berkeley
- **Performance Characteristics of the I960CA Superscalar Microprocessor**
Steven McGeady, Intel Corporation, Santa Clara, CA

12:30–2:00 Lunch

2:00–2:30 Special Memorial Presentation on Dr. Robert Noyce

Dr. Gordon Moore, Chairman of the Board, Intel Corp., Santa Clara, CA

2:45–4:15 Video and Graphics Session Chair: Hasan Alkhatib

- **A Video Compression Chip Set**
Peter Ruetz, LSI Logic Corp., Milpitas, CA
- **C_Cube CL550 Image Coprocessor**
Steven Purcell, C_Cube Corporation, San Jose, CA
- **DVI and 1750 Chip Set**
Sanjay Vinekar, Intel Corporation, Princeton, NJ

4:15–4:45 Soda Break

4:45–5:45 Packaging Session Chair: Theresa Meng

- **Dense Stack**
John Forthun, Dense-Pac Microsystems, Inc., Garden Grove, CA
- **Silicon Multichip Modules**
Donald Benson, nChip Inc., San Jose, CA

5:50–6:50 Floating Point Session Chair: Theresa Meng

- **A 120 MFLOP CMOS Floating Point Unit**
Alan Quek, Weitek Corporation, San Jose, CA
- **A 100MHz Floating Point/Integer Processor**
Gregory Taylor, Bipolar Integrated Technology, Inc., Beaverton, OR

**7:30 Banquet with Speaker John Doerr, General Partner with Kleiner Perkins
Caufield & Byers**

Organizing Committee for the HOT Chips Symposium II:

Hasan Alkhatib, General Chair, Santa Clara University

John Crawford, Program
Intel Corporation

Alan Jay Smith, Program
U. C. Berkeley

Robert Stewart, Treasurer,
Past General Chair
Stewart Research Enterprises

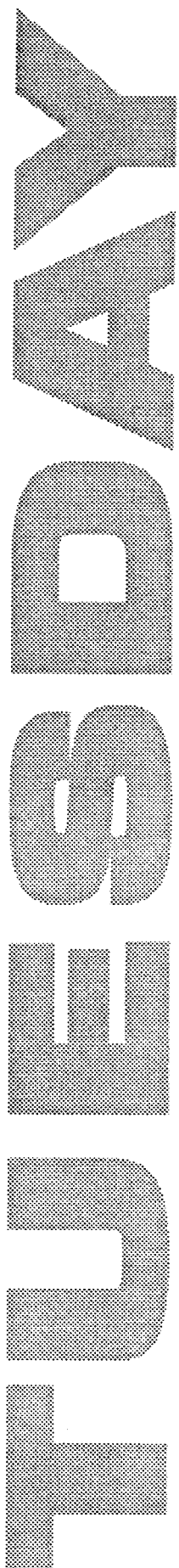
Nam Ling, Registration
Santa Clara University

Doug Marquardt, Local
Arrangements, Santa Clara Univ.
Cynthia Wirtz, Publications
CrossCheck Technology
Martin Freeman, TCMM Member
Philips Research Center

Andy Goforth, Publicity
NASA Ames Research Center
Glen Langdon, TCMM Chair &
Publicity, U. C. Santa Cruz
Stacy Peña, Publicity
CrossCheck Technology
Jack Grimes, Past Prog. Co-Chair
Mass Microsystems

August 21, 1990 – Mayer Theater, Santa Clara University

On-site registration 8:00 – 8:45 a. m.



8:45–10:45 High Performance Microprocessors - II

Session Chair: Martin Freeman

- **96-bit General Purpose IEEE 754 Floating Point Dual Port Processor**
Terry Schultz, Motorola, Anaheim, CA
- **A Single Chip Integer VLIW Processor Core**
Gerrit Slavenburg, Philips Research, Sunnyvale, CA
- **The Clipper Super Scalar CMOS Chip Set**
Howard Sachs, Integraph Corporation, Palo Alto, CA
- **Experience with the 1860 CPU**
John Casey, Hauppauge Corporation, Hauppauge, NY

10:45–11:15 Coffee Break

11:15–12:45 Systolic and Arrays Session Chair: John Crawford

- **The Touchstone DELTA Prototype: A 30 GigaFlop Scalable Parallel Computer**
Justin Rattner and others, Intel Corporation, Aloha, OR
- **100 MOP LIW Microprocessor for Multicomputers**
Craig Peterson, iWarp Group, Intel Corporation, Aloha, OR
- **DataWave - a Data Driven Video Signal Array Processor**
Ulrich Schmidt, ITT Intermetall, Freiburg, Germany

12:45–2:15 Lunch

2:15–3:45 Routing and Interconnect Session Chair: Forest Baskett

- **Caltech Mesh-Routing Chips**
Charles Seitz, California Institute of Technology, Pasadena, CA
- **Get Off the Bus and Call a Taxi**
Paul Scott, Advanced Micro Devices, Sunnyvale, CA
- **Hot Rod: 1Gbit/sec. Data Communications**
Johnathan Zierk, Gazelle Microcircuits, Inc., Santa Clara, CA

3:45–4:15 Soda Break

4:15–5:45 IBM's New Superscalar RISC Session Chair: David Patterson

- **RISC System/6000 Architecture, Implementation, and Performance**
B. Bakoglu and R. Oehler, IBM Watson Res. Ctr., Yorktown Heights, NY
- **Compiling for the RISC System/6000 Branch Unit**
Martin Hopkins, IBM Watson Research Ctr., Yorktown Heights, NY
- **RISC System/6000 Floating Point Unit**
Troy N. Hicks, Oscar R. Mitchell, and Richard E. Fry, IBM Advanced Workstation Div., Austin, TX

5:45 Closing Remarks

Program Committee for the HOT Chips Symposium II:

Alan Jay Smith and John Crawford, Program Co-Chairs

Forest Baskett
Silicon Graphics Computer Sys.

John Hennessy
Stanford University

David Ditzel
Sun Microsystems

Teresa Meng
Stanford University

David Patterson
U. C. Berkeley

Mario Tokoro
Keio University, Japan