mips RISC ARCHITECTURE

ARCHITECTURE TOPICS

INTRODUCTION

INSTRUCTION SET

PIPELINE EFFICIENCY

STREAMING

SUMMARY

ARCHITECTURAL PHILOSOPHY

BUILD ON OUR EXPERIENCE

RISC: SMART SOFTWARE, JUST ENOUGH HARDWARE

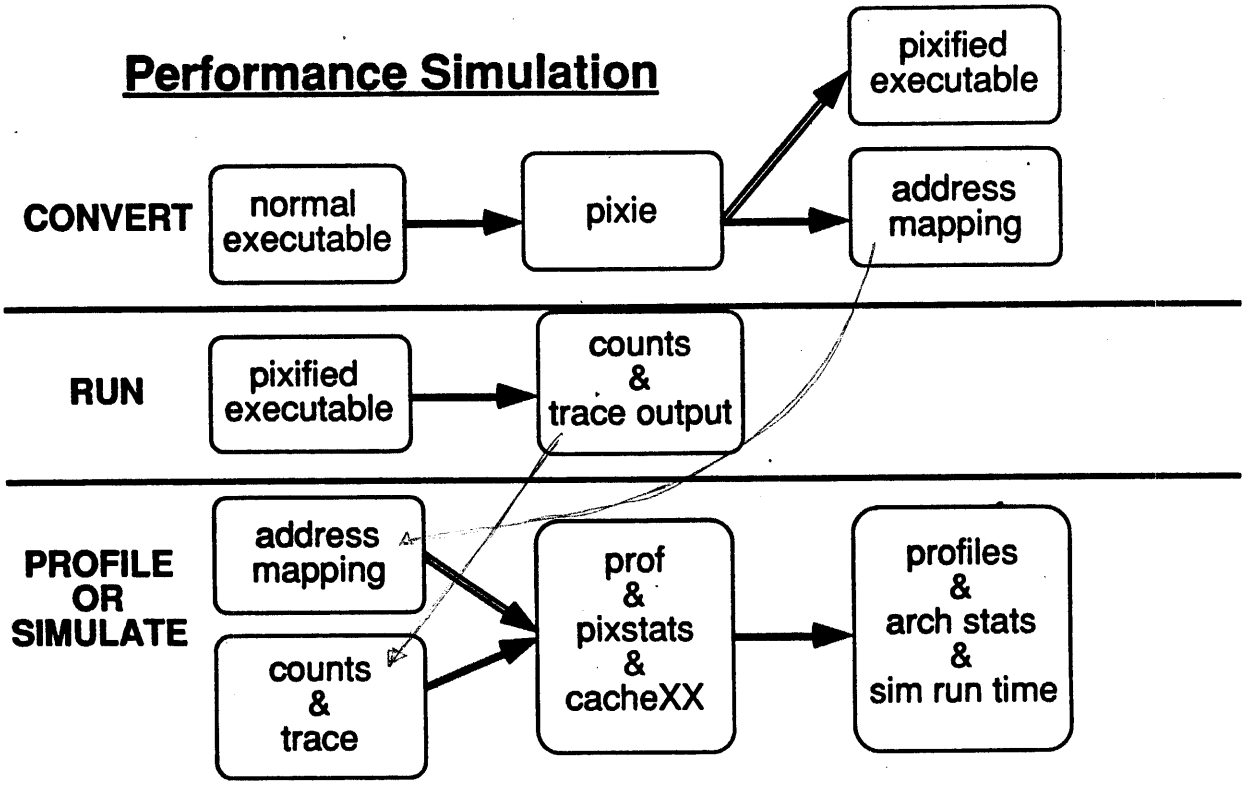
FAST STATIC RAMS
- **KEY ENABLING TECHNOLOGY**
- **TAILOR TO USE AVAILABLE DEVICES**
- **LEVERAGE THE IC INDUSTRY**

PARTITION APPROPRIATELY FOR THE TECHNOLOGY
- **CMOS, BiCMOS, ECL**

EXTENSIVE SIMULATION OF ALTERNATIVES

MEASURE GAIN BEFORE ADDING FEATURE

Performance Simulation



THE BEST PERFORMANCE ANALYSIS SYSTEM AVAILABLE ANYWHERE

Simulation Correlation

	11/780 Secs	MIPS M Instr	M/1000 Simulation t	M/1000 Real t	% Error
5diff	246.4	248.1			
as1	6.5	5.2	0.5	0.5	0
ccom	10.2	8.4	0.9	0.9	0
compress	12.7	17.4	1.7	1.9	-10
doducd	96.3	53.1	7.0	6.7	+4
espresso	382.6	494.7	38.6	38.6	0
gnuchess	124.0	138.8	13.0	13.2	-1.5
hspice	186.3	141.9	15.0	15.1	-0.66
tex	140.0	134.6	17.0	16.9	+0.66
ugen	9.8	6.9	0.6	0.7	-14
uopt	121.2	106.4	9.3	9.4	-1.0
wolf	185.4	147.6	15.0	15.3	-2
yacc	101.1	125.9	9.2	9.3	-1
mean	110.2	111.1			

← LARGE , REAL PROGRAMS

CLOSE MATCH BETWEEN SIMULATION AND REAL SYSTEM

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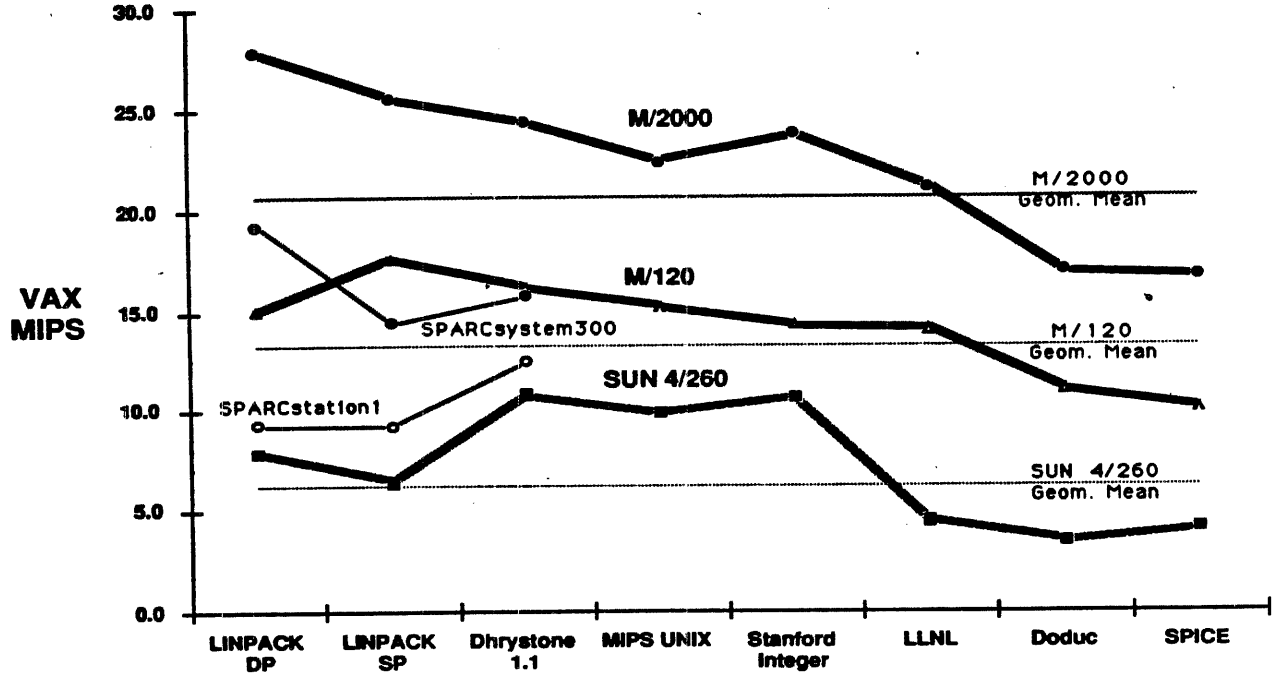
PERFORMANCE RELATIVE TO A VAX 11/780



6/1/89DC

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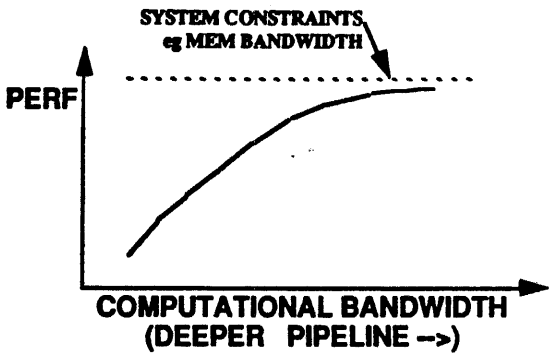
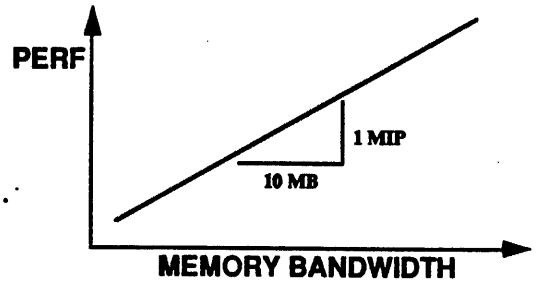
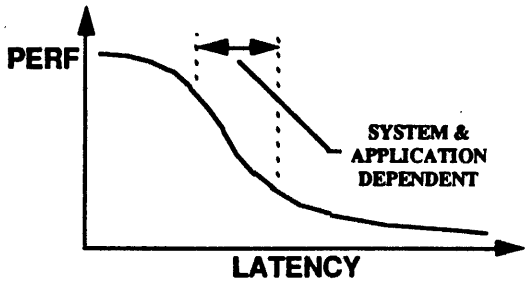
WHAT AFFECTS PERFORMANCE MOST?







... MIPS EMPHASIZES LOW LATENCY

KEY ARCHITECTURAL FEATURES

FASTEST EFFECTIVE LOAD/STORE/BRANCH OF ANY RISC

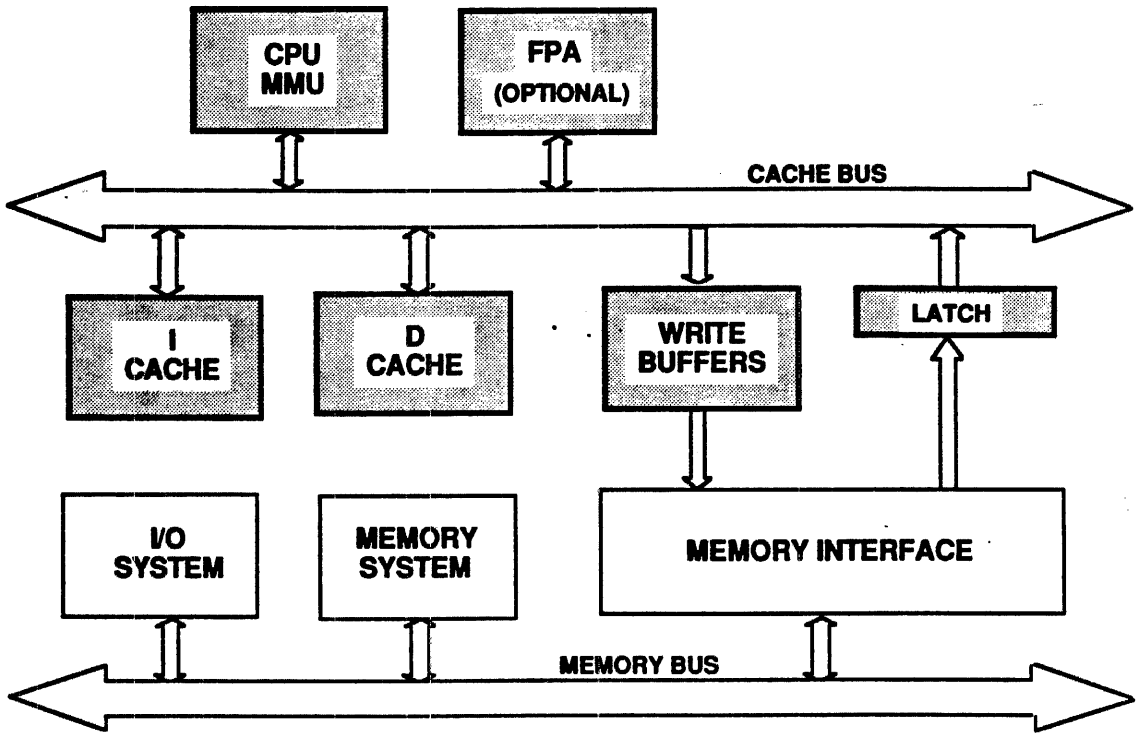
OUTSTANDING SYSTEM SOFTWARE SUPPORT

HIGHEST MEMORY BANDWIDTH

USES STANDARD SRAMS FOR COST EFFECTIVE CACHE

HARDWARE SUPPORT FOR MULTIPROCESSING

SYSTEM BLOCK DIAGRAM



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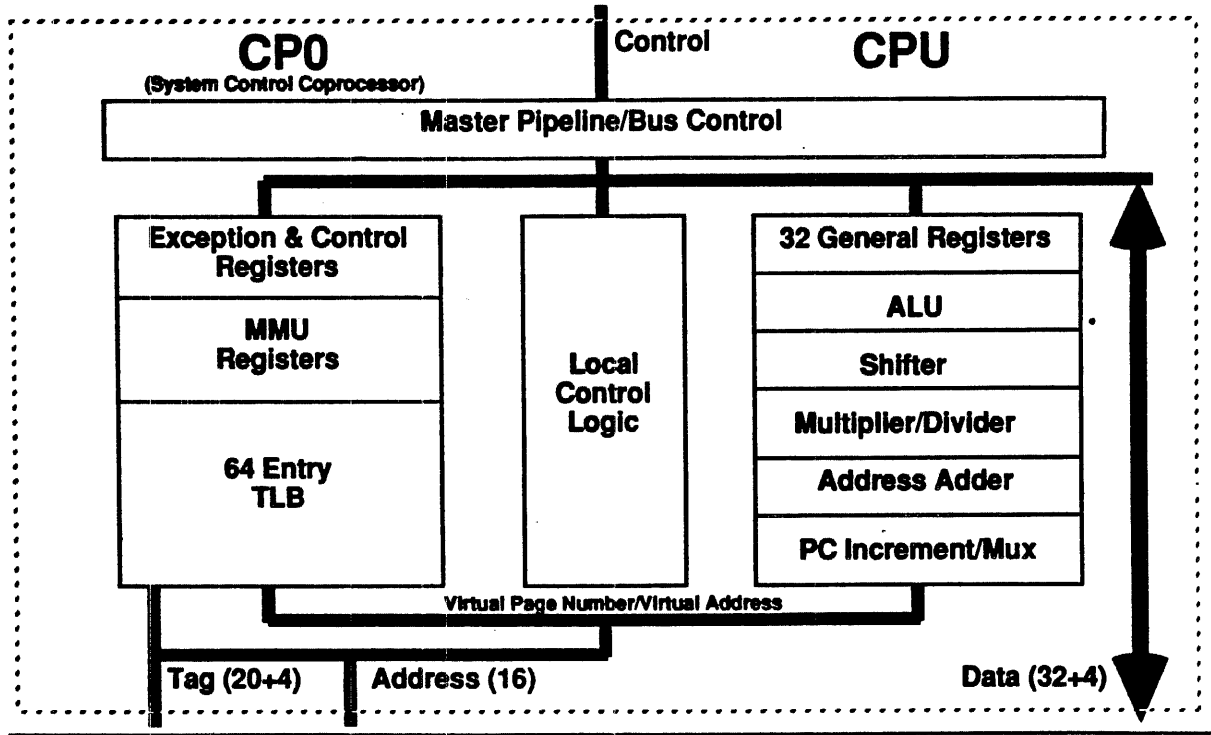
R3000 BLOCK DIAGRAM



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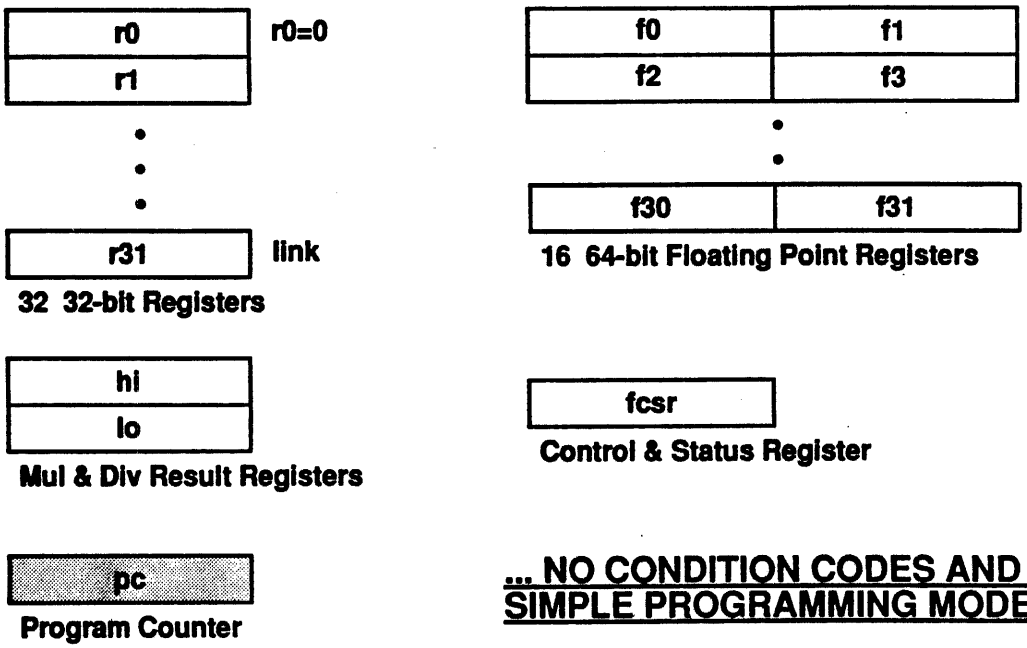
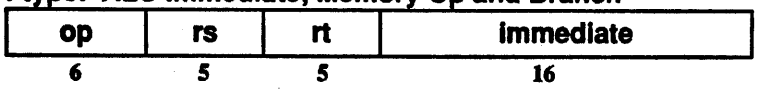
User State Registers



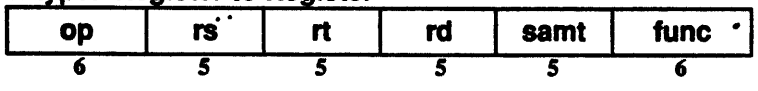
... NO CONDITION CODES AND A SIMPLE PROGRAMMING MODEL.

Instruction Formats

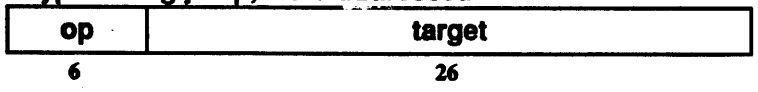
I-type: ALU immediate, Memory Op and Branch



R-type: Register to Register



J-type: Long jump, word addressed



SIMPLE, REGULAR FORMATS ALLOW FAST DECODE & PIPELINE

INSTRUCTION SET

LOAD/STORE

Byte addressed, Bi-endian
Word, Halfword, Byte
Signed, Unsigned
Unaligned References
Base + 16 bit Offset

ALU

Add, Sub, Logicals
- Rd:=Rs op Rt, 3 register operations
- Rt:=Rs op I, 2 register + 16 bit immediate

Impact of compare & branch on arithmatic ops:
- Add/Sub with no trap, unsigned arith
- Add/Sub with trap, ADA, Pascal, LISP

BRANCHES

No Condition Codes; Compare and Branch
One Instruction Branch on:
- A<0, A≤0, A>0, A≥0, A=B, A≠B

When needed, two instructions for:
- A<B, A≤B, A>B, A≥B

Branches execute next instruction before branching
Also Jumps: J, JAL, JR, JALR

MULTIPLY/DIVIDE

Compile most constants with shft/add/sub
Hardware accelerates remaining
- 12 cycle mult, 35 cycle divide

64 bit product, or quotient/remainder

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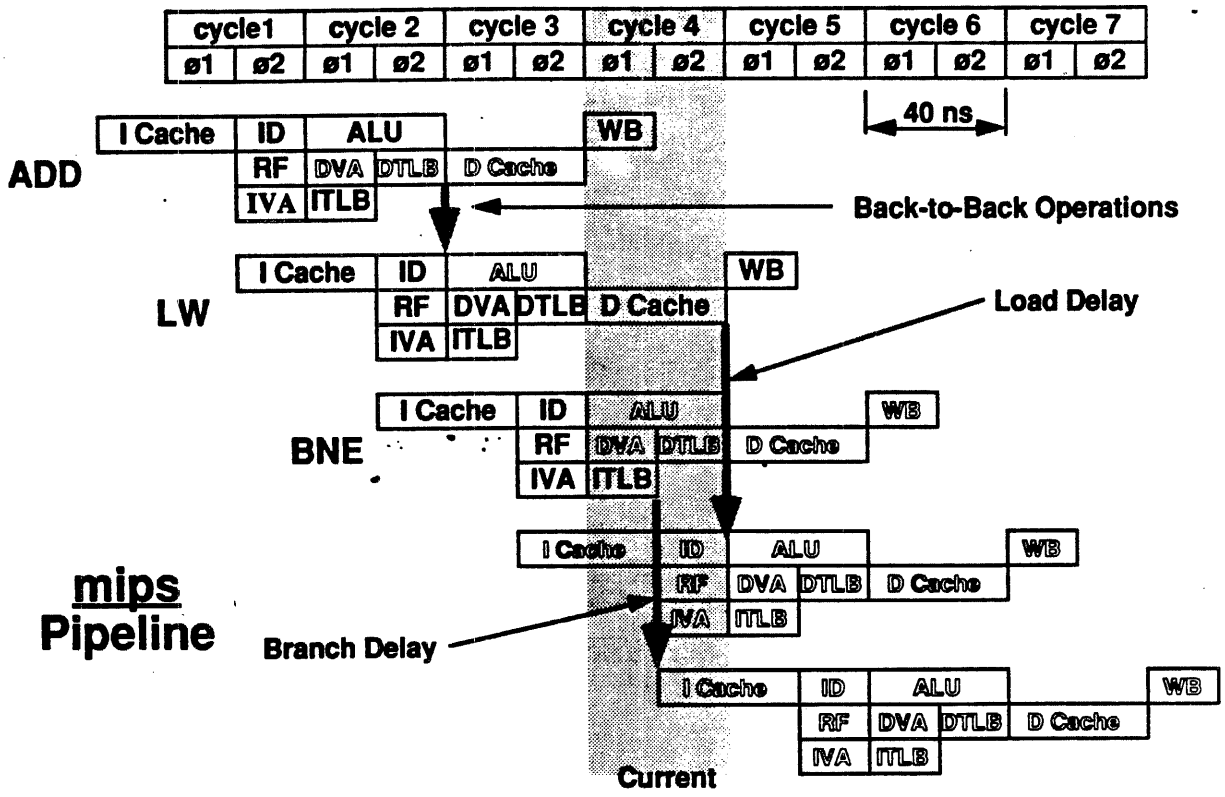
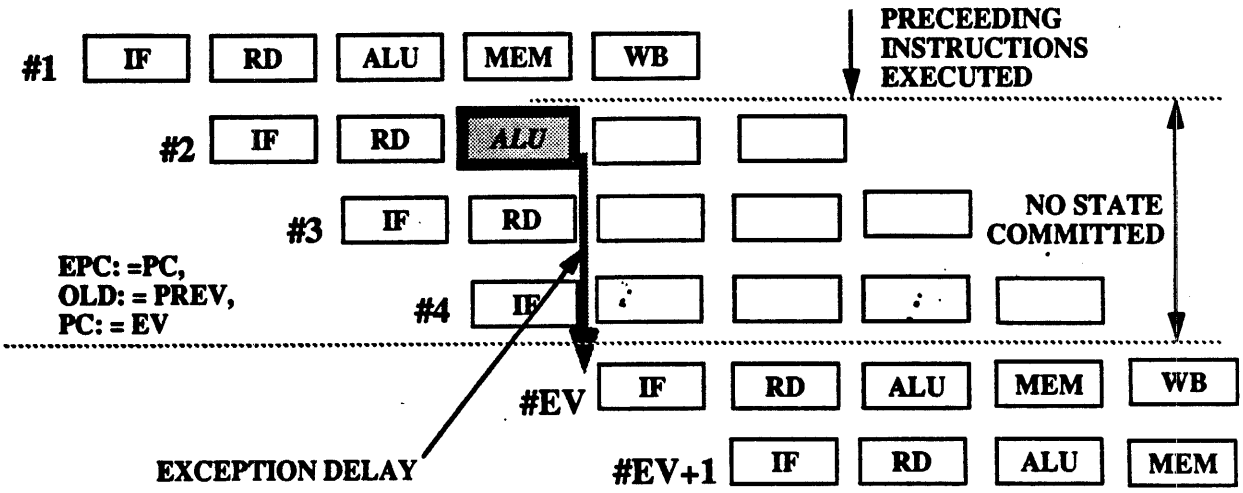


PRECISE EXCEPTION HANDLING



CRITICAL PIPELINE & SYSTEM DESIGN FACTOR
HARDWARE MAKES ALL EXCEPTIONS PRECISE

PERFORMANCE COMPARISONS

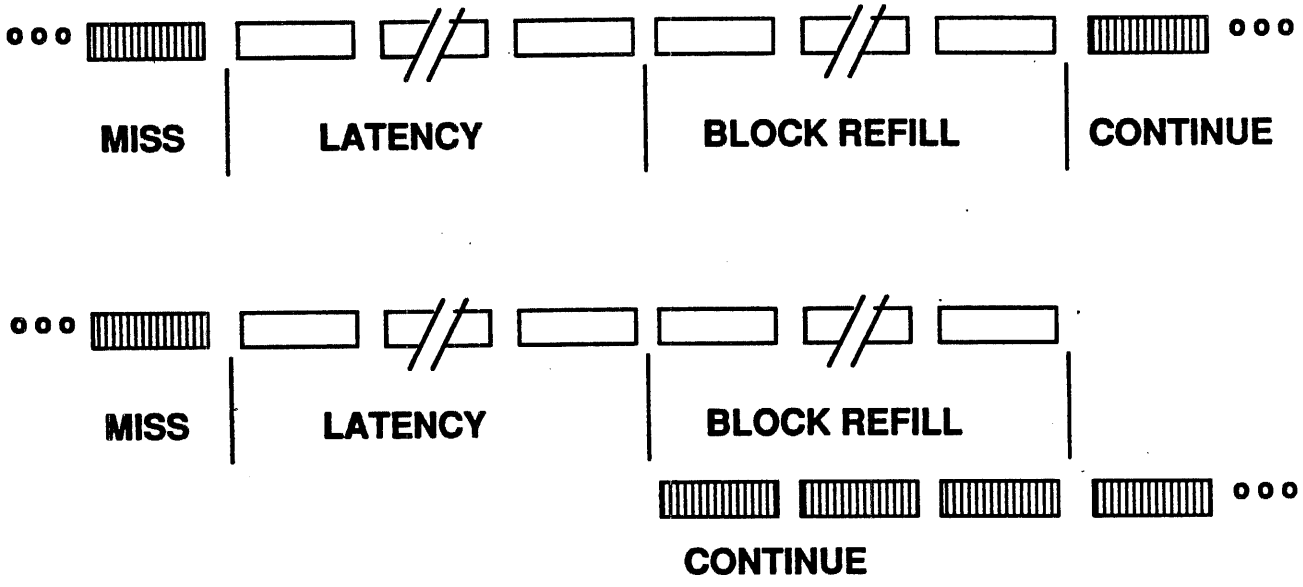
PROC	CLOCK (MHz)	WDS/CYC (4 Bytes)	BNDWTH (MB/sec)	CPI (MHz/VUP)	VAX-MIPS (VUPs)
68020	20	1/3	27	7.0	3
68030	20	1/2	33	6.0	4
68030 (Sun3/200)	25	1/3	40	6.2	4
80386	25	1/2	50	6.0	5
68030	33	1/2	67	5.5	6
SPARC (Sun4/200)	16	1/1	67	2.1	8
29000	25	2/1	200	2.0	12
R2000 (M/120)	16	2/1	134	1.5	12
88000	20	2/1	160	1.5	13
SPARC	33	1/1	134	2.1	16
88000	25	2/1	200	1.5	17
R3000 (M/2000)	25	2/1	200	1.2	20

MIPS BLOCK REFILL

- AMORTIZE COST OF LATENCY OVER MULTIPLE WORDS
- CPU HARDWARE CONTROLS THE TRANSFER
- CHOICE OF 4, 8, 16, or 32 WORD BLOCK SIZES
- SEPARATE INSTRUCTION AND DATA BLOCK SIZES
- DESIRABLE TO TUNE BLOCK SIZE TO SYSTEM DESIGN, INCREASE BLOCK SIZE AS LATENCY TO MEMORY INCREASES
- BLOCK REFILL HAS LARGE IMPACT ON HIT RATE, SECOND ONLY TO TOTAL CACHE SIZE

FLEXIBILITY

MIPS INSTRUCTION STREAMING



MIPS INSTRUCTION STREAMING

- BEGIN EXECUTION WHEN INSTRUCTION ARRIVES, ISSUE INSTRUCTION IN SAME CYCLE AS CACHE WRITE

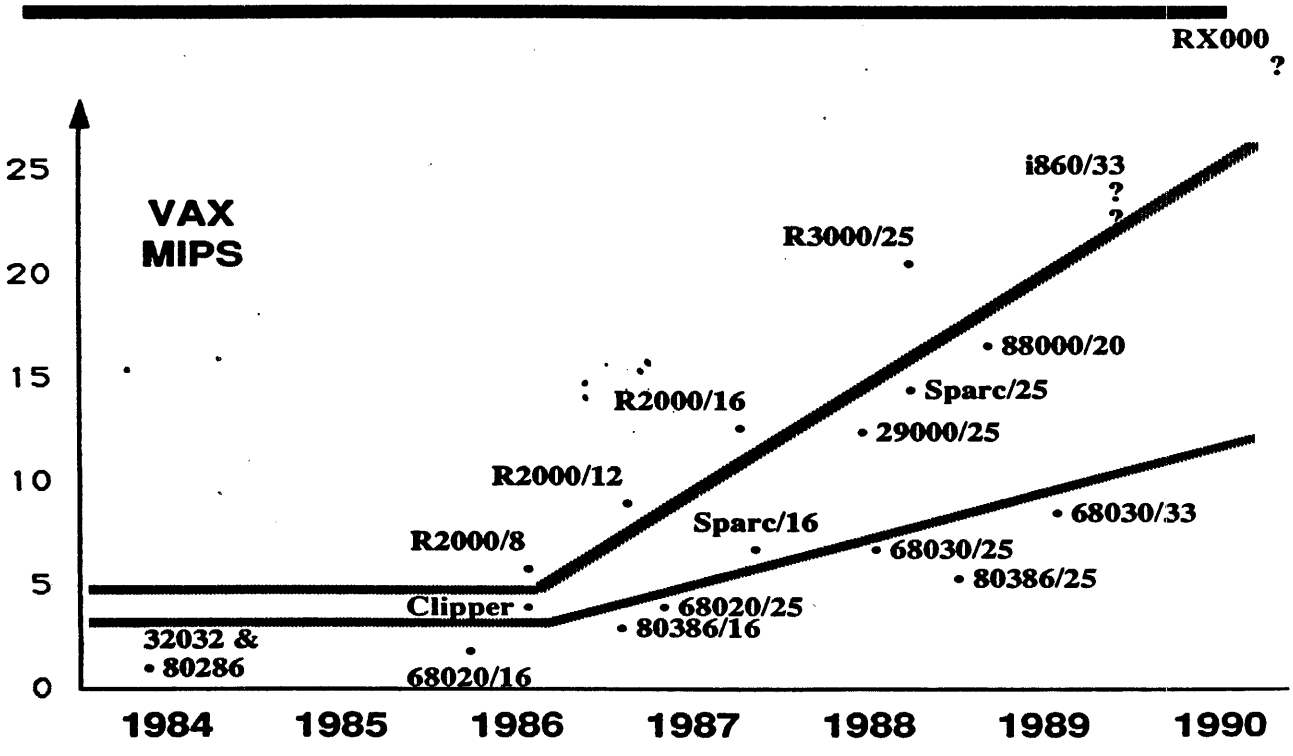
- 70% OF INSTRUCTION MISSES START AT BLOCK BOUNDRY, GREATEST BENEFIT TO STREAMING INSTRUCTIONS

- MAXIMUM EXECUTION SPEED MATCHES MAX MAIN MEMORY BANDWIDTH, 100MB/SEC

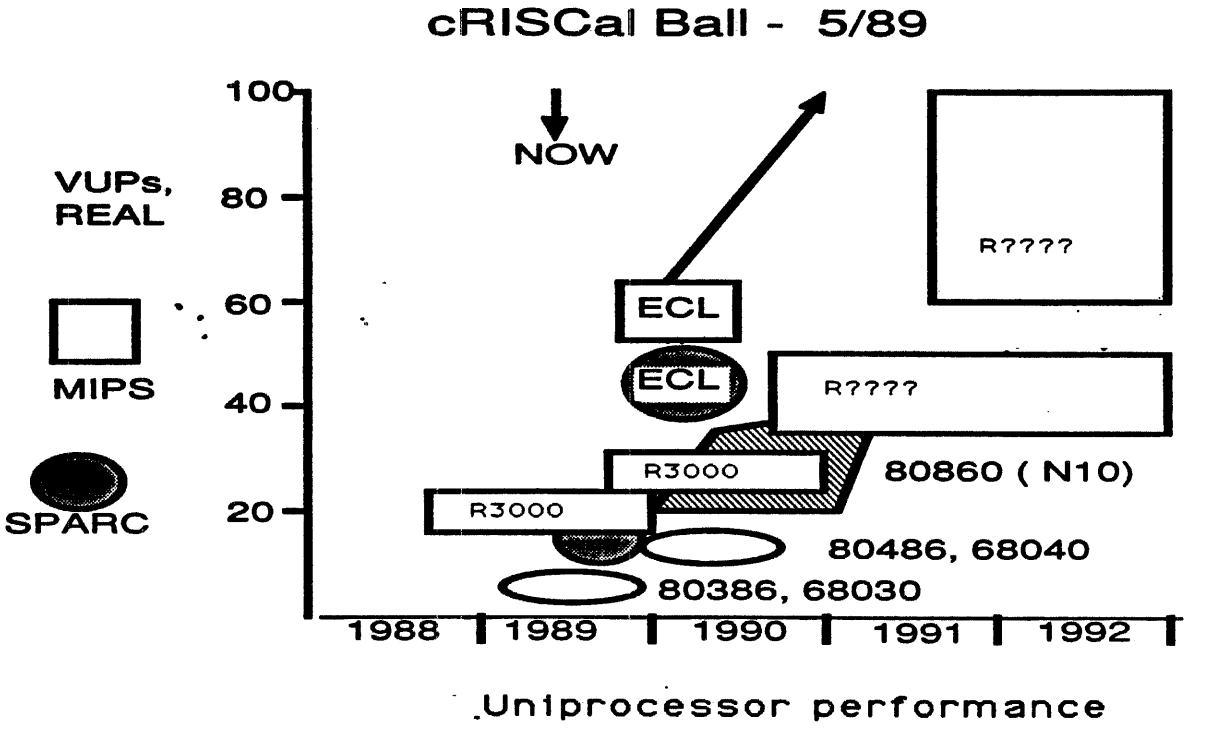
- 5% NET GAIN - vs SYSTEM WITHOUT INSTRUCTION STREAMING

HIGHER PERFORMANCE

mips RISComponents™ LEAD



Where are we today?



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