SPRING HILL (NNP-I 1000) – DESIGN GOALS

- Best in class perf/power efficiency for major data center inference workloads
  - 4.8 TOPs/W
- 5X power scaling for performance boost
  - 10-50W
- Achieve high degree of programmability w/o compromising perf/power efficiency
  - Drive AI innovation with on die Intel Architecture cores
- Data Center at Scale
  - Comprehensive set of RAS features to allow seamless deployment in existing data centers
- Highly capable SW stack supporting all major DL frameworks

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INTRODUCING – SPRING HILL (NNP-I)

Intel 10nm Process Technology

Dynamic power management and FIVR technology

Intel IA cores with AVX and VNNI

PCIe Gen 3 EP x4/x8

SNC IA Core

| ICE | ICE | ICE |
| ICE | ICE | ICE |

Cache Coherency Fabric 24MB shared cache

24MB LLC for fast Inter ICE & IA data data sharing

4x32, 2x64 LPDDR4x 4.2 GT/s, IB ECC

DDR IO (LPDDR4)

SNC IA Core

| ICE | ICE | ICE |
| ICE | ICE | ICE |

12x Inference Compute Engines (ICE)

HW based sync for ICE to ICE communication

Feature	SoC
TOPs (INT8)	48 – 92
TDP	10-50w
TOPs/w	2.0-4.8 TOPs/w
Inference Engines (ICE)	10-12 ICEs
Total SRAM	75MB
DRAM BW	68 GB/s

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ICE - INFERENCE COMPUTE ENGINE

- **Deep Learning compute grid**
  - 4K MAC (int8) per cycle
  - Scalable support: FP16, INT8, INT 4/2/1
  - Large internal SRAMs for power efficiency
  - Non-linear ops & Pooling
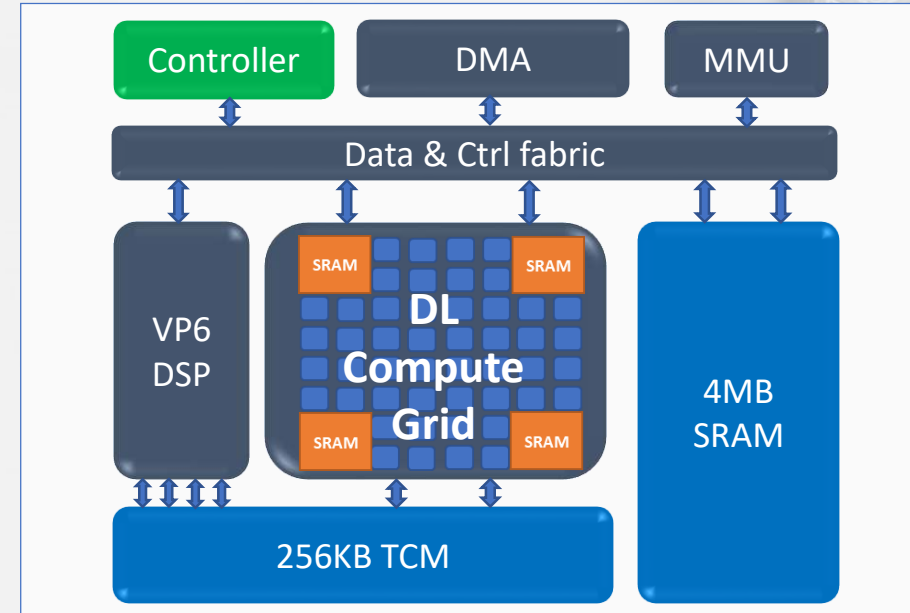- **Programmable vector processor**
  - High throughput: 5 VLIW 512b
  - Extended NN support (FP16/16b/8b)
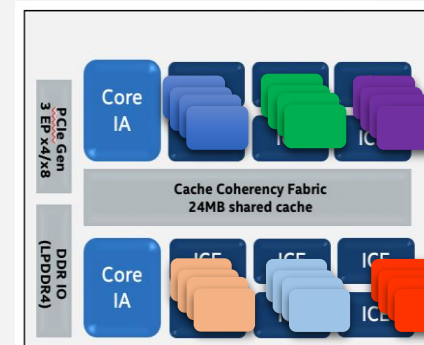- **High BW data memory access**
  - Dedicated DMA – optimized for DL
  - Compression/decompression unit- support for sparse weights
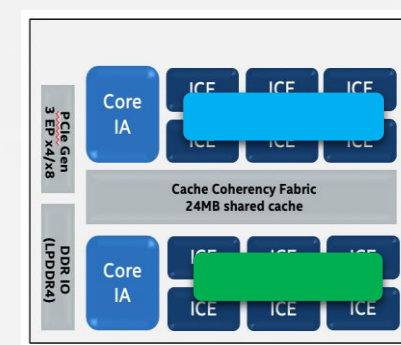- **Large Local SRAM**
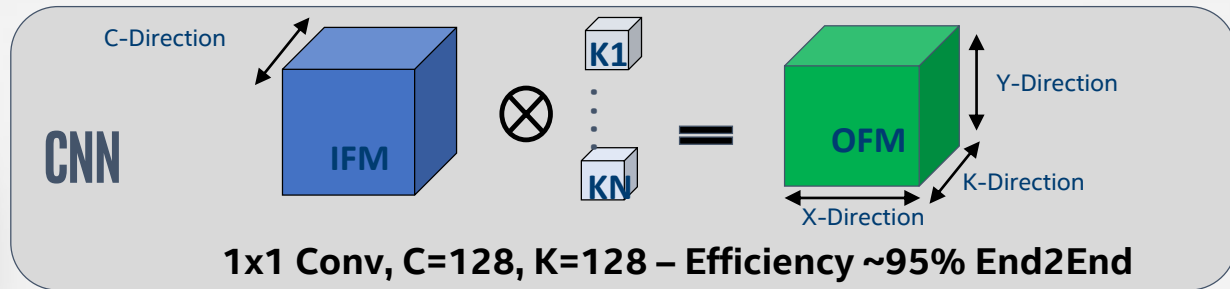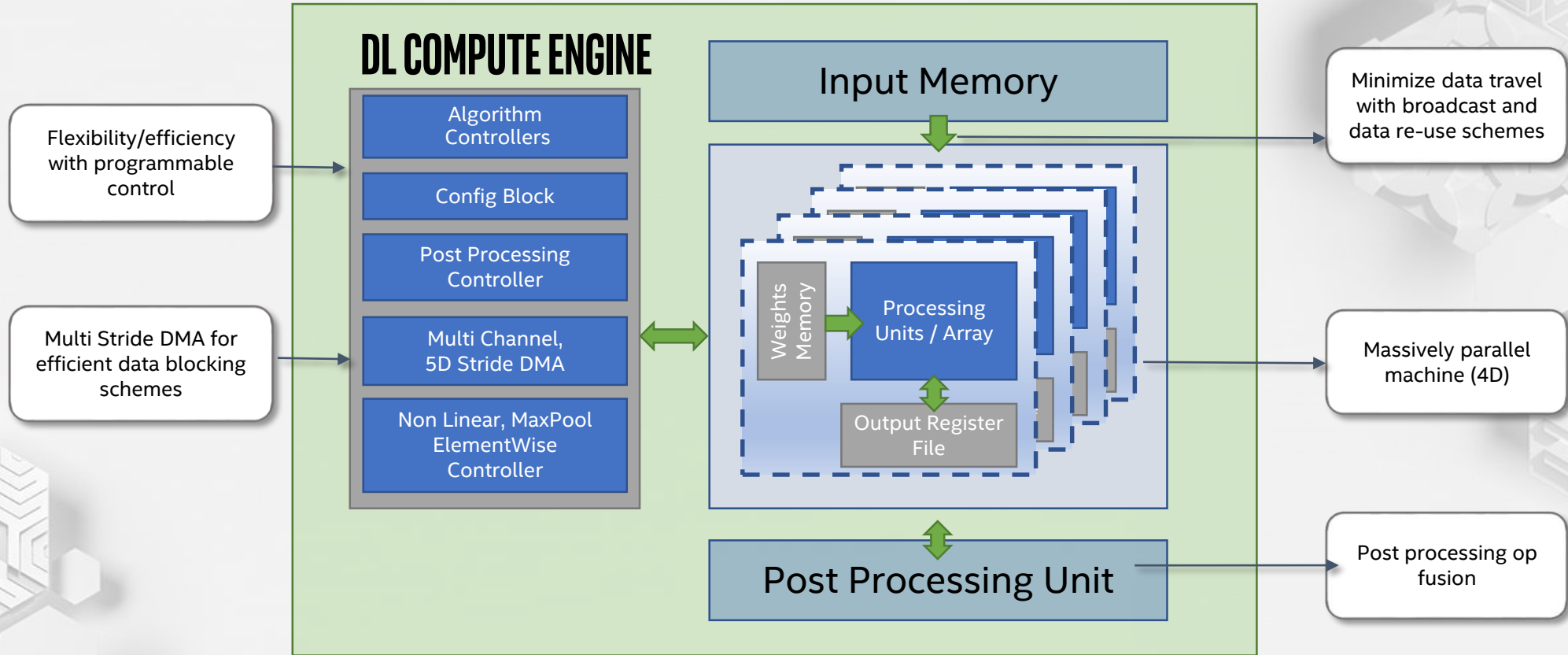 - Persistent data and/or storage of temporal data

Optimized for throughput
batch: 4x6 (or 1X12)

Optimized for latency
batch: 1x2

DL COMPUTE GRID

DL COMPUTE ENGINE

Flexibility/efficiency with programmable control

Multi Stride DMA for efficient data blocking schemes

- Algorithm Controllers
- Config Block
- Post Processing Controller
- Multi Channel, 5D Stride DMA
- Non Linear, MaxPool ElementWise Controller

Input Memory

Weights Memory

Processing Units / Array

Output Register File

Post Processing Unit

Minimize data travel with broadcast and data re-use schemes

Massively parallel machine (4D)

Post processing op fusion

CNN

C-Direction

IFM ⊗ K1 ⋮ KN = OFM

Y-Direction
K-Direction
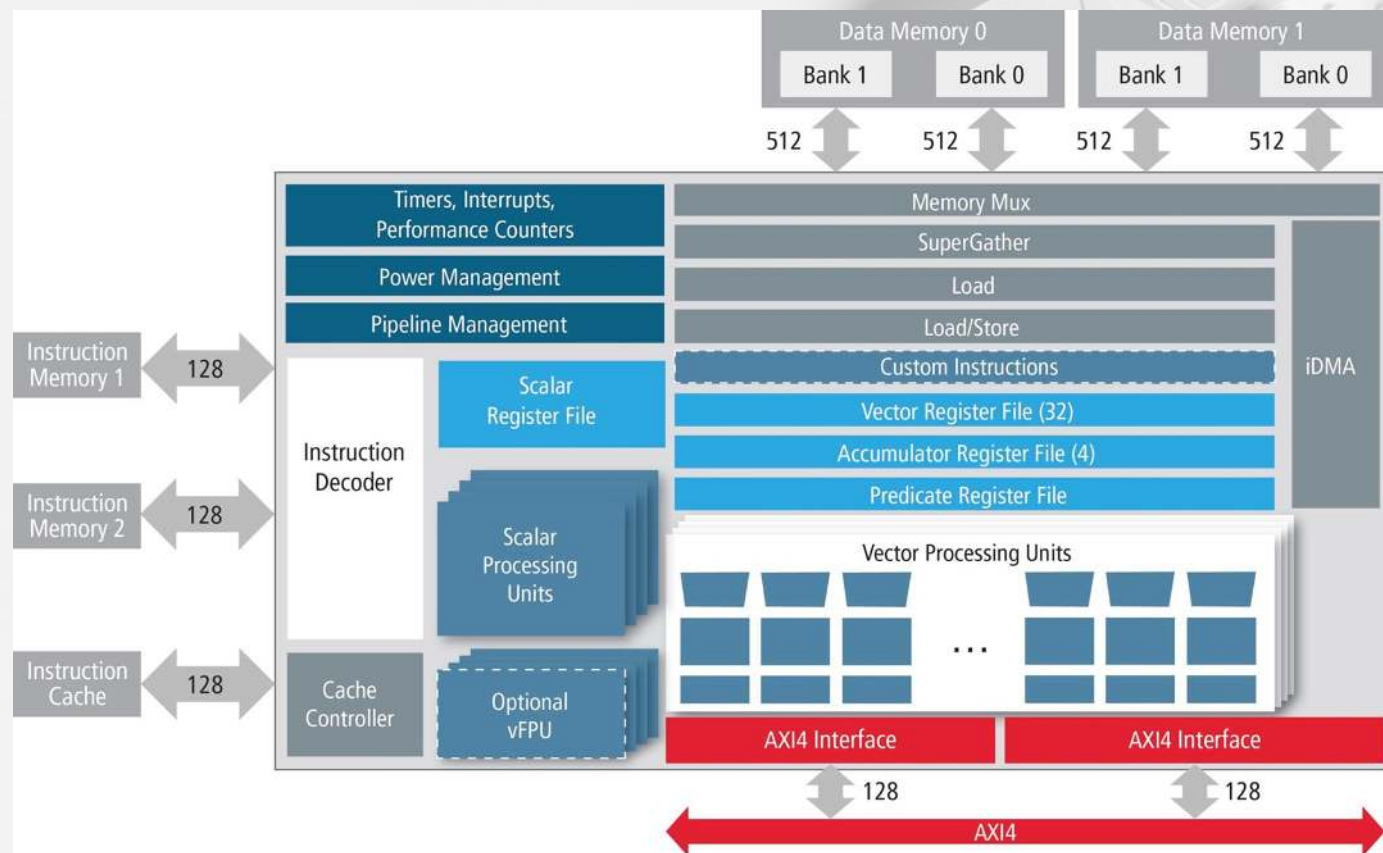X-Direction

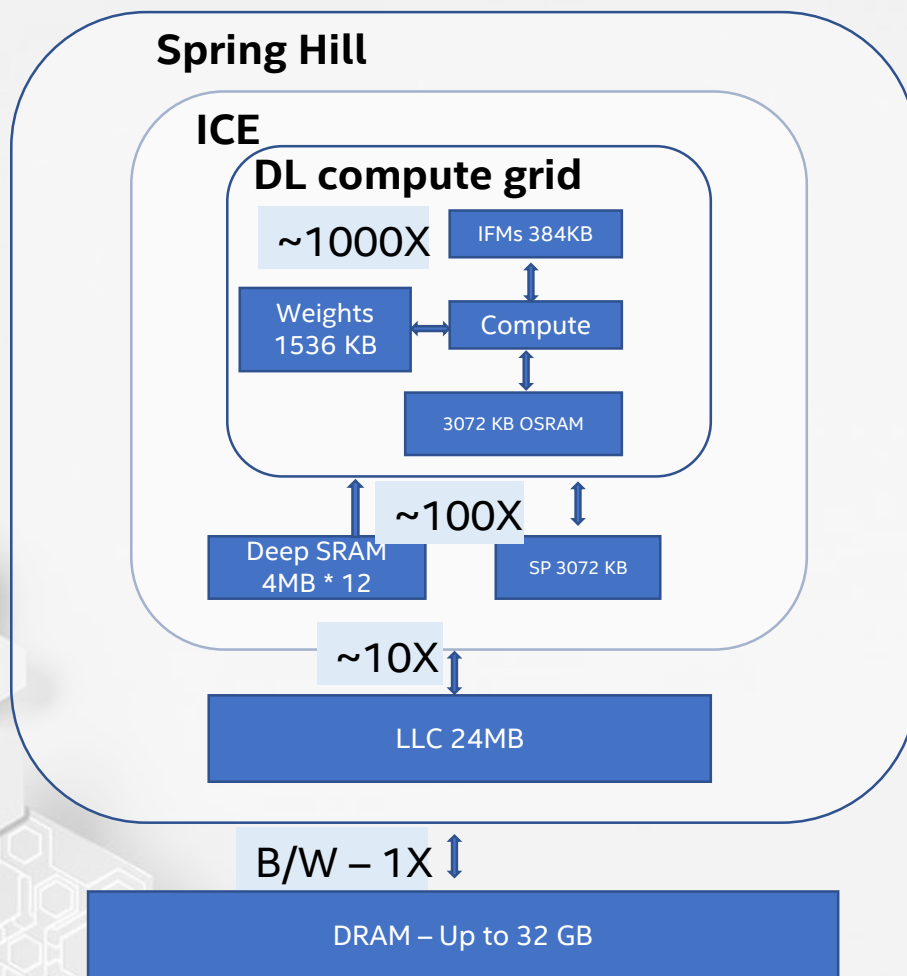**1x1 Conv, C=128, K=128 – Efficiency ~95% End2End**

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THE VECTOR PROCESSING ENGINE

- Tensilica Vision P6 DSP
  - 5 VLIW, 512b vector
  - 2 Vector Load ports
  - Scatter/gather engine
  - Data type: Int8,16,32, FP16
- Fully programmable
- Full bi-directional pipeline with the DL compute Grid
  - Shared local memory
  - HW Sync. between producer and consumer

MEMORY ORGANIZATION

Spring Hill

ICE

DL compute grid

~1000X

IFMs 384KB

Weights 1536 KB

Compute

3072 KB OSRAM

~100X

Deep SRAM 4MB * 12

SP 3072 KB

~10X

LLC 24MB

B/W – 1X

DRAM – Up to 32 GB

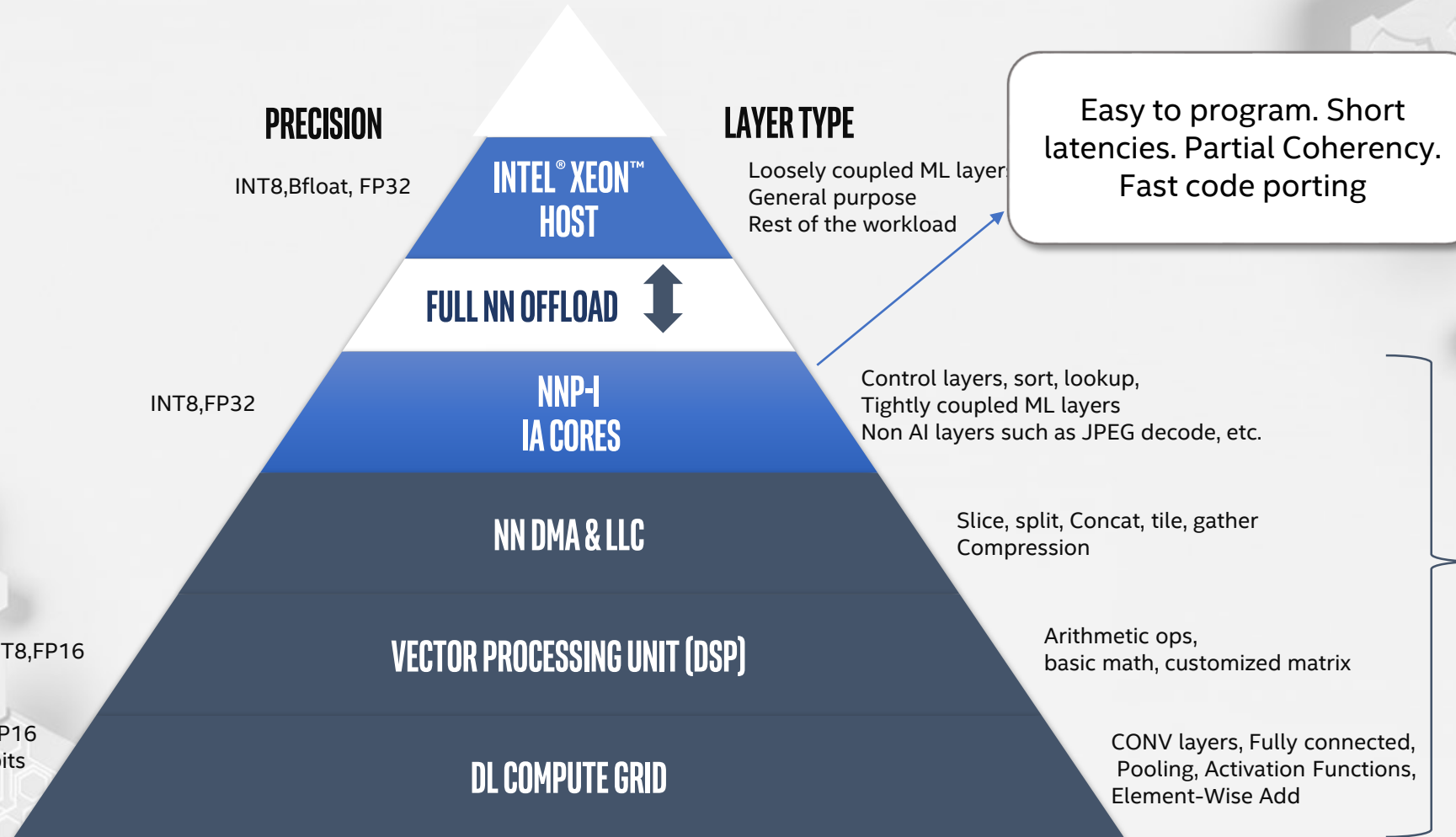| Power management				
PCIe Phy	PCIe EP	ICE Sync	IB ECC	MC
IA SNC	3MB	3MB	IA SNC	
ICE / ICE RS	3MB	3MB	ICE / ICE RS	
ICE / AI RS	3MB	3MB	ICE / ICE RS	
ICE / ICE RS	3MB	3MB	ICE / ICE RS	

- 24MB LLC
  - Organized in 8X3MB slices
  - Shared data (ICE-to-ICE, ICE-to-IA)
  - Optimized for DL inference workloads
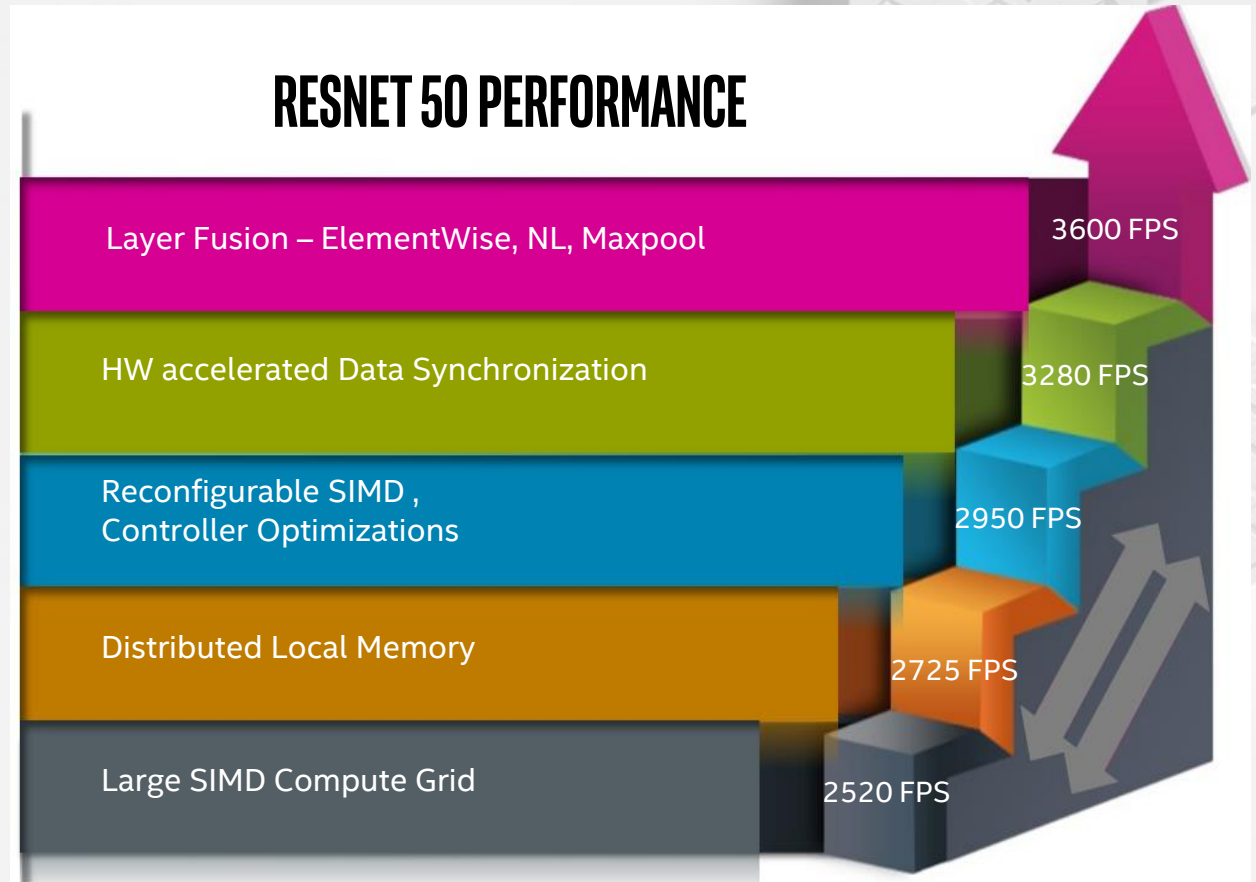
(intel)

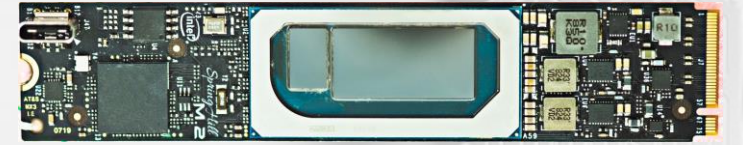# PROGRAMMING FLEXIBILITY AND WORKLOAD DECOMPOSITION

SPH (NNP-I 1000) PERFORMANCE

- **ResNet50**
  - 3600 Inferences Per Second (IPS)
  - @10W (SOC level)
  - 360 Images/Sec/W
  - 2→12 AI cores 5.85x
- **Performance/W – 4.8 TOPs/W**
- **Additional preliminary performance disclosure with MLPerf 0.5 Submission**

RESNET 50 PERFORMANCE

Layer Fusion – ElementWise, NL, Maxpool — 3600 FPS

HW accelerated Data Synchronization — 3280 FPS

Reconfigurable SIMD, Controller Optimizations — 2950 FPS

Distributed Local Memory — 2725 FPS

Large SIMD Compute Grid — 2520 FPS

SUMMARY

- Best in class perf/power efficiency for major data center inference workloads

- Scalable performance at wide power range

- Achieve high degree of programmability w/o compromising perf/power efficiency

- Data Center at Scale

- Spring hill solution -- Silicon and SW stack – sampling with definitional partners/customers on multiple real-life topologies

- Next 2 generations in planning/design

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