

# FUTURE INTEL® XEON® SCALABLE PROCESSOR (CODENAME: CASCADE LAKE-SP)

Akhilesh Kumar, Sailesh Kottapalli, Ian M Steiner, Bob Valentine, Israel Hirsh, Geetha Vedaraman, Lily P Looi, Mohamed Arafa, Andy Rudoff, Sreenivas Mandava, Bahaa Fahim, Sujal A Vora

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### Outline

- Intel<sup>®</sup> Xeon<sup>®</sup> Scalable Processor Roadmap
- Focus Areas for Cascade Lake-SP
  - Instruction Enhancement for AI/Deep Learning Inference
  - Intel<sup>®</sup> Optane<sup>™</sup> DC Persistent Memory
  - Side Channel Mitigations
- Wrap up

#### First Generation Intel<sup>®</sup> Xeon<sup>®</sup> Scalable Processor Introduced in July 2017

- Skylake-SP core microarchitecture with data center specific enhancements
- Intel<sup>®</sup> AVX-512 with 32 DP flops per cycle per core
- Data center optimized cache hierarchy 1MB L2 per core, non-inclusive L3

- New Intel<sup>®</sup> Mesh architecture
- Enhanced 6 channel memory subsystem
- 48 lanes of PCIe Gen3 with integrated DMA, NTB, and VMD devices
- New Intel<sup>®</sup> Ultra Path Interconnect (Intel<sup>®</sup> UPI)

Features	Intel <sup>®</sup> Xeon <sup>®</sup> Scalable Processor
Cores and Threads Per CPU	Up to 28 cores and 56 threads
Last-level Cache (LLC)	Up to 38.5 MB (non-inclusive)
QPI/UPI Speed (GT/s)	Up to 3x UPI @ 10.4 GT/s
PCIe* Lanes/ Controllers	Up to 48 / 12 / PCIe 3.0 (2.5, 5, 8 GT/s)
Memory Population	Up to 6 channels of up to 2 RDIMMs, LRDIMMs, or 3DS LRDIMMs
Max Memory Speed	Up to 2666 MHz



#### Foundation for Accelerating Data Center Innovations



### Next Step in the Intel® Xeon® Scalable Processor

Cascade Lake CPU is designed to be compatible with first-gen Intel<sup>®</sup> Xeon<sup>®</sup> Scalable platform

- Same core count, cache size, and I/O speeds as first-gen
- Process tuning, frequency push, targeted performance improvements
- Architectural improvements through targeted instruction set enhancements
- New platform capabilities with support for Intel<sup>®</sup> Optane<sup>™</sup> DC persistent memory
- Hardware enhancements for protection against side-channel methods





# **AI/DEEP LEARNING ENHANCEMENTS**

# AI/Deep Learning Software Optimizations

#### on first generation Intel® Xeon® Scalable Processor



(1) Up to 5.4X performance improvement with software optimizations on Caffe Resnet-50 in 10 months with 2 socket Intel® Xeon® Scalable Processor, Configuration Details 1, 2. Performance measurements were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system.

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# **Neural Machine Translation Software Optimization**

#### on first generation Intel<sup>®</sup> Xeon<sup>®</sup> Scalable Processor

MxNet Amazon\* C5 (Intel<sup>®</sup> Xeon<sup>®</sup> Processor) NMT<sup>1</sup>(German to English)



#### Configuration Details 3 4

Performance measurements were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system. Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel does not optimize to intel microprocessors. These optimizations include SSE2, SSE3, and SSE3 instruction sets and other optimizations. Intel does not maintacture do y file. Microprocessors devices of any optimizations in this product are intended to use with Intel microprocessors. These optimizations not specific to Intel microprocessors. Seesended to find microprocessors. Seesended to find microprocessors. Seesended to find microprocessors. Seesended to find microprocessors. Seesended to intel microprocessors. Seesended to intel microprocessors. Seesended to the applicable product are intended to use with Intel microprocessors. Seesended to intel microprocessors. Seesended to the mapplicable product are intended to use with Intel microprocessors. Seesended to intel microprocessors. Seesended to intel microprocessors. Seesended to the microprocessors. Seesended to the applicable product are intended to use with Intel microprocessors. Seesended to intel microprocessors. Seesended to the microprocessors. Seesended to intel microprocessors. Seesended noré complete information visit: http://www.intel.com/performance Source: Intel measured as of May



### **Cascade Lake Vector Neural Network Instructions**

Vector Neural Network Instruction (VNNI) on Cascade Lake accelerates Deep Learning and AI inference workloads

- VNNI : A new set of Intel<sup>®</sup> Advanced Vector Extension (Intel<sup>®</sup> AVX-512) instructions
  - 8-bit (int8) new instruction (VPDPBUSD)
    - Fuses 3 instructions in inner convolution loop using int8 data type
  - 16-bit (int16) new instruction (VPDPWSSD)
    - Fuses 2 instructions in inner convolution loop using int16 data type



#### AI/DL Inference Enhancements on INT16 with VNNI



#### New instructions for accelerating AI on Intel® Xeon® Scalable processors using int16 data





## AI/DL Inference Enhancements on INT8 with VNNI



#### New instructions for accelerating AI on Intel® Xeon® Scalable processors using int8 data





## VNNI Per Core Throughput

Vector Elements Processed per Cycle on Different Data Types



Performance measurements were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectre" and "Meltdown." Implementation of these updates may make these results inapplicable to your device or system. Optimization Notice: Intel's completes may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE3, SSE3, instruction sets and other optimizations, theil does not optimize to the same degree for non-Intel microprocessors for optimizations include to set. Sec4, and SSE3 instruction sets and other optimizations, theil does not optimized to address exploits referred to use with microprocessors. These optimizations in other optimized to address exploits include SSE3, SSE3, and SSE3 instruction sets and other optimizations. Intel does not optimized to address exploits referred to use with microprocessors. These optimizations in other optimized to address exploits not set optimized to address exploits and the notions in other optimized to address exploits and the optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions in other optimized to address exploits and the notions and the notions in other optimized to address exploits and the notions in oth

## Inference Throughput with VNNI



1 Intel® Optimization for Caffe Resnet-50 performance does not necessarily represent other Framework performance. 2 Based on Intel internal testing: 1X (7/11/2017), 2.8X (1/19/2018) and 5.4X (7/26/2018) performance improvement based on Intel® Optimization for Caffe Resnet-50 inference throughput performance on Intel® Xeon® Scalable Processor. 3 11X (7/25/2018) Results have been estimated using internal Intel analysis, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance. Performance results are based on testing as of 7/11/2017(1x), 1/19/2018(2.4X) & 7/26/2018(5.4) and may not reflect all publically available security update. See configuration disclosure for details (config 5). No product can be absolutely secure. Optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessors-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations on specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Other names and brands may be claimed as the property of others.



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# **REIMAGINING DATA CENTER MEMORY HIERARCHY**

## Growing Gap Between Memory Hierarchy

Limitations to traditional architecture impede unified data management



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## Growing Gap Between Memory Hierarchy

Limitations to traditional architecture impede unified data management



### **Intel Innovations Address These Gaps**



Future Intel<sup>®</sup> Xeon<sup>®</sup> Scalable Processor – Hot Chips 2018







#### Supported on future Intel® Xeon® Scalable Processors (Cascade Lake)





#### Intel<sup>®</sup> Optane<sup>™</sup> DC Persistent Memory Hardware Interface



- DDR4 electrical and physical interface with proprietary protocol extensions
- Memory channel can be shared between DDR4 and Intel<sup>®</sup> Optane<sup>™</sup> DC persistent memory modules
  - Enables systems to support greater than 3TB of system memory per CPU socket
- Cache line size accesses
- Idle latency close to DDR4 DIMMs

arformance measurements were obtained prior to implementation of recent software patches and firmware updates intended to address exploits referred to as "Spectr" and "Meltdown." Implementation of hese updates may make these results inapplicable to your device or system. Simitation Notifice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations in this product are not unjour to hese optimizations not specific to Intel microprocessors. These optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microprocessors. Program and "Meltown." error optimization on microprocessors for manufactured by Miel. Microprocessors: Pleaker are not unjour use with Intel microprocessors. Certain optimizations not specific to Intel microprocessors. Pleaker are resolved for Intel microprocessors. Pleaker are not unjour use with Intel microprocessors. These optimizations not specific to Intel microprocessors. Pleaker are resolved for Intel microprocessors. Pleaker are not unjour and volt mose and workloads used in performance tests, may have been optimized for performance only on Intel microprocessors. Pleaker and workloads used in performance only on Intel microprocessors. Performance tests, such as SYS mark and Moleser and volt mose and workloads used in performance on the information on and performance only on Intel microprocessors. Performance on the processor and the information on the performance on the processor. The measured using in the performance on the



### Hardware Interface: Persistence Domain



## The SNIA NVM Programming Model





## The Persistent Memory Development Kit - pmdk

#### PMDK is a collection of libraries

- Developers pull only what they need
  - Low level programming support
  - Transaction APIs
- Fully validated
- Performance tuned

**Open source & product neutral** 

#### software.intel.com/pmem





### Usage Example: High Performance Storage



Results have been estimated based on tests conducted on pre-production systems, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to www.intel.com/benchmarks.



# Usage Example: Data Replication with Persistent Memory over Fabric



Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to www.intel.com/benchmarks. "Three 9s and five 9s availability assumes bi-weekly maintenance restarts.

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# HARDWARE MITIGATION FOR SIDE CHANNEL

#### **Cascade Lake Mitigations for Side-Channel Methods**

#### Cascade Lake implements hardware mitigations against targeted side-channel methods

Variant	Side-Channel Method	Mitigation on Cascade Lake
Variant 1	Bounds Check Bypass	OS/VMM
Variant 2	Branch Target Injection	Hardware + OS/VMM
Variant 3	Rogue Data Cache Load	Hardware
Variant 3a	Rogue System Register Read	Firmware
Variant 4	Speculative Store Bypass	Firmware + OS/VMM or runtime
	L1 Terminal Fault	Hardware

# Cascade Lake SP expected to provide higher performance over software mitigations available for existing products

For additional information related to security updates and side channel methods on Intel<sup>®</sup> products, please visit <u>https://www.intel.com/content/www/us/en/architecture-and-technology/facts-about-side-channel-analysis-and-intel-products.html</u>



## Future Intel<sup>®</sup> Xeon<sup>®</sup> Scalable Processor (Codename: Cascade Lake-SP)





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#### Config Details for Skylake Inference throughput (March 2018)





#### Config 2

#### Config Details for Skylake Inference throughput (April 2018)

	tensorflow	tensorflow	tensorflow	tensorflow	tensorflow	tensorflow	tensorflow	tensorflow	tensorflow	mxnet	mxnet	mxnet	mxnet	mxnet	mxnet
	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: master	branch: mas er
Framework	version: 024aecf4149 41e11eb643e29ceed 3e1c47a115ad	version: 024aecf4149 41e11eb643e29ceed 3e1c47a115ad	version: 024aecf414 941e11eb643e29cee d3e1c47a115ad	version: 024aecf414 941e11eb643e29cee d3e1c47a115ad	version: 024aecf414 941e11eb643e29cee d3e1c47a115ad	version: 024aecf41 4941e11eb643e29 ceed3e1c47a115ad	version: 024aecf41 4941e11eb643e29 ceed3e1c47a115ad	version: 024aecf41 4941e11eb643e29 ceed3e1c47a115a d	version: 024aecf41 4941e11eb643e2 9ceed3e1c47a115 ad	version: fdb5664 900682c8173a50 826acec8b1111d 9cd6f	version: fdb56649 00682c8173a508 26acec8b1111d9c d6f	version: fbbc080d 47323dbc23eef4a 1453452624cea8 59b	version: 9a0d0 028695cbc355 3ffadf3537b10 03bb0006c4	version: fdb566 4900682c8173 a50826acec8b 1111d9cd6f	version: fdb 664900682 8173a5082 acec8b1111 9cd6f
Sockets	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Processor	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores	Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 2 cores								
BIOS	SE5C620.86B.00.01.0 004.071220170215	SE5C620.86B.00.01.0 004.071220170215	SE5C620.86B.00.01. 0004.071220170215	SE5C620.86B.00.01. 00004.071220170215	SE5C620.86B.00.01. 0004.071220170215	SE5C620.86B.00.0 1.0004.071220170 215	SE5C620.86B.00.0 1.0004.071220170 215	SE5C620.86B.00.0 1.0004.071220170 215	SE5C620.86B.00.0 1.0004.07122017 0215	SE5C620.86B.00. 01.0004.0712201 70215	SE5C620.86B.00.0 1.0004.07122017 0215	SE5C620.86B.00.0 1.0004.07122017 0215	SE5C620.86B.0 0.01.0004.071 220170215	SE5C620.86B.0 0.01.0004.071 220170215	SE5C620.86 .00.01.0004. 712201702 5
Enabled Cores	56	56	56	56	56	56	56	56	56	56	56	56	56	56	56
Slots	12	12	12	12	12	12	12	12	12	12	12	12	12	12	12
Total Memory	376.28GB	376.46GB	376.46GB	376.46GB	376.46GB	376.46GB	376.46GB	376.46GB	376.46GB	376.28GB	376.28GB	376.28GB	376.28GB	376.28GB	376.28GB
Memory Configuration	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz	12slots / 32 GB / 2666 MHz
Aemory Comments	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron	Micron
Disks	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB	sda RS3WC080 HDD 744.1GB,sd RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB						
OS	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	CentOS Linux- 7.3.1611-Core	Ubuntu-16.04- xenial	Ubuntu-16.04- xenial	Ubuntu-16.04- xenial	Ubuntu-16.04- xenial	Ubuntu-16.04- xenial	Ubuntu- 16.04-xenia
Hyper Threading	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Turbo	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Topology	resnet 50 v1	resnet 50 v1	resnet 50 v1	vgg16	vgg16	vgg16	inception v3	inception v3	inception v3	resnet 50 v2	vgg16	vgg16	inception v3	inception v3	inception v
Batchsize	1	64	128	1	64	128	1	64	128	1.64.128	1	64, 128	1	64	128
nstances/ Streams on 2 sockets	8	8	8	8	8	8	8	8	8	1	1	1	1	1	1
Dataset	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	NoDataLayer	Imagenet	Imagenet	NoDataLayer	Imagenet	NoDataLayer	Imagenet
Engine	MKLDNN version: e0bfcaa7fcb2 b1e1558f5f0676933c 1db807a729	MKLDNN version: e0bfcaa7fcb2 b1e1558f5f0676933c 1db807a729	MKLDNN version: e0bfcaa7fcb 2b1e1558f5f067693 3c1db807a729	MKLDNN version: e0bfcaa7fcb 2b1e1558f5f067693 3c1db807a729	MKLDNN version: e0bfcaa7fcb 2b1e1558f5f067693 3c1db807a729	MKLDNN version: e0bfcaa7fc b2b1e1558f5f0676 933c1db807a729	MKLDNN version: e0bfcaa7fc b2b1e1558f5f0676 933c1db807a729	MKLDNN version: e0bfcaa7fc b2b1e1558f5f067 6933c1db807a729	MKLDNN version: e0bfcaa7f cb2b1e1558f5f06 76933c1db807a7 29	MKLDNN version: f5218ff4f d2d16d13aada2e 632afd18f2514fe e3	MKLDNN version: f5218ff4f d2d16d13aada2e 632afd18f2514fe e3	MKLDNN version: 283c4a8c 24b4e1dea05fbc7 941594a7375bab ad1	MKLDNN version: f5218f f4fd2d16d13aa da2e632afd18f 2514fee3	MKLDNN version: f5218f f4fd2d16d13aa da2e632afd18f 2514fee3	MKLDNN version: f52 8ff4fd2d16d 3aada2e632 fd18f2514fe 3
Kernel version	3.10.0- 693.11.6.el7.x86_64	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	4.4.0-109-generic	3.10.0- 693.11.6.el7.x86_ 64	3.10.0- 693.11.6.el7.x86_ 64	3.10.0- 693.11.6.el7.x86_ 64	3.10.0- 693.11.6.el7.x8 6_64	3.10.0- 693.11.6.el7.x8 6_64	3.10.0- 693.11.6.el7 86_64



# Configuration details of Amazon EC2 C5.18xlarge 1 node systems

Benchmark Segment	AI/ML
Benchmark type	Inference
Benchmark Metric	Sentence/Sec
Framework	Official mxnet
Topology	GNMT(sockeye)
# of Nodes	1
Platform	Amazon EC2 C5.18xlarge instance
Sockets	25
Processor	Intel <sup>®</sup> Xeon <sup>®</sup> Platinum 8124M CPU @ 3.00GHz (Skylake)
BIOS	N/A
Enabled Cores	18 cores / socket
Platform	N/A
Slots	N/A
Total Memory	144GB
Memory Configuration	N/A
SSD	EBS Optimized 200GB, Provisioned IOPS SSD
OS	Red Hat 7.2 (HVM) Amazon Elastic Network Adapter (ENA) Up to 10 Gbps of aggregate network bandwidth
Network Configurations	Installed Enhanced Networking with ENA on Centos Placed the all instances in the same placement
НТ	ON
Turbo	ON
Computer Type	Server



#### Configuration details of Amazon EC2 C5.18xlarge 1 node systems

Framework Version	mxnet mkldnn : <u>https://github.com/apache/incubator-mxnet/</u> 4950f6649e329b23a1efdc40aaa25260d47b4195
Topology Version	GNMT: <a href="https://github.com/awslabs/sockeye/tree/master/tutorials/wmt">https://github.com/awslabs/sockeye/tree/master/tutorials/wmt</a>
Batch size	GNMT:1 2 8 16 32 64 128
Dataset, version	GNMT: WMT 2017 ( <u>http://data.statmt.org/wmt17/translation-task/preprocessed/</u> )
MKLDNN	F5218ff4fd2d16d13aada2e632afd18f2514fee3
MKL	Version: parallel_studio_xe_2018_update1 http://registrationcenterdownload.intel.com/akdlm/irc_nas/tec/12374/parallel_studio_xe_2018_ update1_cluster_edition_online.tgz
Compiler	g++: 4.8.5 gcc: 7.2.1

#### Configuration Details for Inference Throughput with VNNI

#### 1x inference throughput improvement in July 2017:

Tested by Intel as of July 11<sup>th</sup> 2017: Platform: 2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to "performance" via intel\_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86\_64. SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gb/s, 25nm, MLC).**Performance measured with**: Environment variables: KMP\_AFFINITY='granularity=fine, compact', OMP\_NUM\_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance. Caffe: (<u>http://github.com/intel/caffe/</u>), revision f96b759f71b2281835f690af267158b82b150b5c. Inference measured with "caffe time --forward\_only" command, training measured with "caffe time" command. For "ConvNet" topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from <a href="https://github.com/intel/caffe/tree/master/models/intel\_optimized\_models">https://github.com/intel/caffe/tree/master/models/intel\_optimized\_models</a> (ResNet-50), and <a href="https://github.com/soumith/convnet\_benchmarks/tree/master/caffe/imagenet\_winners">https://github.com/soumith/convnet\_benchmarks; files were updated to use newer Caffe protoxt format but are functionally equivalent). Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20170425. Caffe run with "numactl -l".

#### 2.8x inference throughput improvement in January 2018:

Tested by Intel as of Jan 19<sup>th</sup> 2018 Processor :2 socket Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores HT ON , Turbo ON Total Memory 376.46GB (12slots / 32 GB / 2666 MHz). CentOS Linux-7.3.1611-Core, SSD sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB , Deep Learning Framework Intel® Optimization for caffe version:f6d01efbe93f70726ea3796a4b89c612365a6341 Topology::resnet\_50\_v1 BIOS:SE5C620.86B.00.01.0009.101920170742 MKLDNN: version: ae00102be506ed0fe2099c6557df2aa88ad57ec1 NoDataLayer. . Datatype:FP32 Batchsize=64 Measured: 652.68 imgs/sec vs Tested by Intel as of July 11<sup>th</sup> 2017: Platform: 2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to "performance" via intel\_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86\_64. SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gb/s, 25nm, MLC).**Performance measured with**: Environment variables: KMP\_AFFINITY='granularity=fine, compact', OMP\_NUM\_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance. Caffe: (http://github.com/intel/caffe/), revision f96b759f71b2281835f690af267158b82b150b5c. Inference measured with "caffe time --forward\_only" command, training measured with "caffe time" command. For "ConvNet" topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from https://github.com/intel/caffe/tree/master/models/intel\_optimized\_models (ResNet-50), and https://github.com/soumith/convnet-benchmarks/tree/master/caffe/imagenet\_winners (ConvNet benchmarks; files were updated to use newer Caffe protoxt format but are functionally equivalent). Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20170425. Caffe run with "numactl -l".

#### Configuration Details for Inference Throughput with VNNI

#### 5.4x inference throughput improvement in August 2018:

Tested by Intel as of measured July 26<sup>th</sup> 2018 :2 socket Intel(R) Xeon(R) Platinum 8180 CPU @ 2.50GHz / 28 cores HT ON , Turbo ON Total Memory 376.46GB (12slots / 32 GB / 2666 MHz). CentOS Linux-7.3.1611-Core, kernel: 3.10.0-862.3.3.el7.x86\_64, SSD sda RS3WC080 HDD 744.1GB,sdb RS3WC080 HDD 1.5TB,sdc RS3WC080 HDD 5.5TB , Deep Learning Framework Intel® Optimization for caffe version:a3d5b022fe026e9092fc7abc7654b1162ab9940d Topology::resnet\_50\_v1 BIOS:SE5C620.86B.00.01.0013.030920180427 MKLDNN: version:464c268e544bae26f9b85a2acb9122c766a4c396 instances: 2 instances : https://software.intel.com/en-us/articles/boosting-deep-learning-training-inference-performance-on-xeon-and-xeon-phi) NoDatasocket:2 (Results on Intel® Xeon® Scalable Processor were measured running multiple instances of the framework. Methodology described hereLayer. Datatype: INT8 Batchsize=64 Measured: 1233.39 imgs/sec vs Tested by Intel as of July 11<sup>th</sup> 2017:2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to "performance" via intel\_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86\_64. SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gb/s, 25nm, MLC).**Performance measured with**: Environment variables: KMP\_AFFINITY='granularity=fine, compact', OMP\_NUM\_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance. Caffe: (http://github.com/intel/caffe/j), revision f96b75971b2281835f690af267158b82b150b5c. Inference measured with "caffe time" -forward\_only" command, training measured with "caffe time" command. For "ConvNet" topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from <u>https://github.com/intel/caffe/tree/master/models/intel\_optimized\_models</u> (ResNet-50). Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20170425. Caffe run with "numactl -l".

#### 11X inference thoughput improvement with CascadeLake:

Future Intel Xeon Scalable processor (codename Cascade Lake) results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance vs Tested by Intel as of July 11<sup>th</sup> 2017: 2S Intel® Xeon® Platinum 8180 CPU @ 2.50GHz (28 cores), HT disabled, turbo disabled, scaling governor set to "performance" via intel\_pstate driver, 384GB DDR4-2666 ECC RAM. CentOS Linux release 7.3.1611 (Core), Linux kernel 3.10.0-514.10.2.el7.x86\_64. SSD: Intel® SSD DC S3700 Series (800GB, 2.5in SATA 6Gb/s, 25nm, MLC).**Performance measured with**: Environment variables: KMP\_AFFINITY='granularity=fine, compact', OMP\_NUM\_THREADS=56, CPU Freq set with cpupower frequency-set -d 2.5G -u 3.8G -g performance. Caffe: (http://github.com/intel/caffe/), revision f96b759f71b2281835f690af267158b82b150b5c. Inference measured with "caffe time --forward\_only" command, training measured with "caffe time" command. For "ConvNet" topologies, dummy dataset was used. For other topologies, data was stored on local storage and cached in memory before training. Topology specs from https://github.com/intel/caffe/tree/master/models/intel\_optimized\_models (ResNet-50),. Intel C++ compiler ver. 17.0.2 20170213, Intel MKL small libraries version 2018.0.20170425. Caffe run with "numactl -l".



